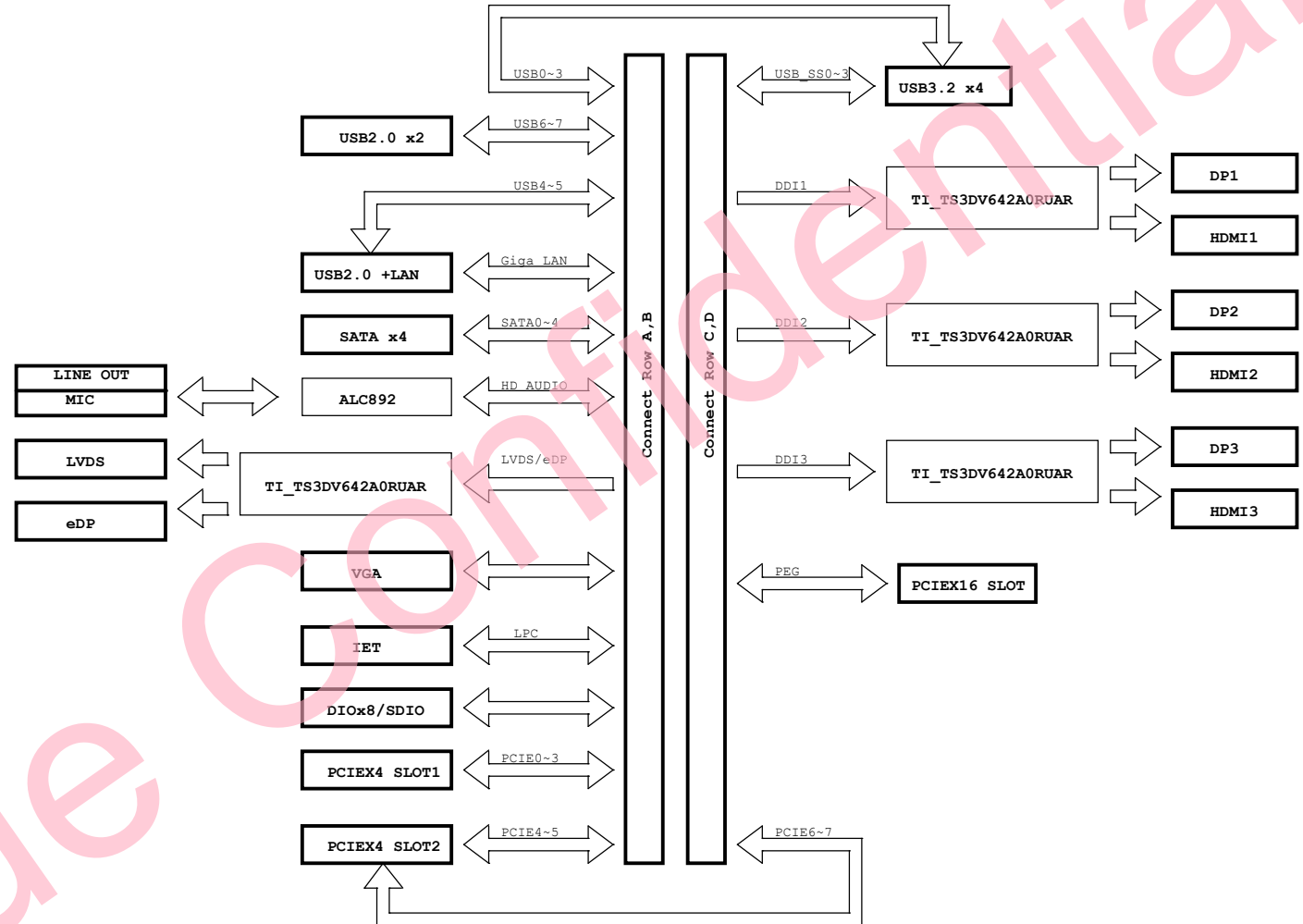
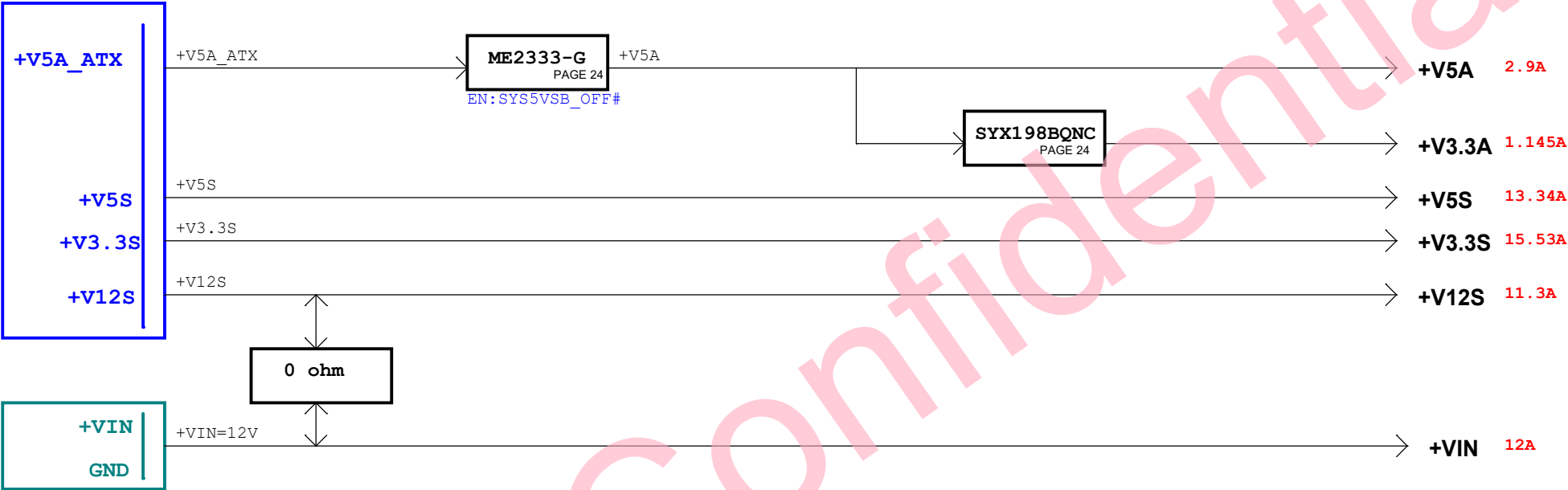


Page	Function
01	BLOCK DIAGRAM
02	Power Delivery Map
03	Clock Distribution
04	Power Sequence
05	Board information
06	COM EXPRESS CONNECTOR
07	DDI1 switch & DP1
08	HDMI1
09	DDI2 switch & DP2
10	HDMI2
11	DDI3 switch & DP3
12	HDMI3
13	LVDS & EDP
14	VGA
15	PCIEX16
16	PCIEX4
17	USB3.2、USB2.0
18	SATA、LAN、SD、DIO
19	SPI、RTC、FAN
20	AUDIO_2CH(ALC892)
21	IET & PORT 80(LPC/ESPI)
22	FPGA
23	CONTROL,SETTING,TEST
24	POWER IN & CONTROL
25	MODIFY HISTORY

BLOCK DIAGRAM



Power Delivery Map



COMexpress	
+VIN	12A
+VCC_5VSB	2A

CPU FAN	
+V12S	1A

System FAN	
+V12S	1A

SDIO	
+V5S	1A

DIO	
+V5S	1A

DDI1 HDMI/DP SWITCH	
+V3.3S	0.05A

DDI2 HDMI/DP SWITCH	
+V3.3S	0.05A

DDI3 HDMI/DP SWITCH	
+V3.3S	0.05A

LVDS/eDP SWITCH	
+V3.3S	0.05A

HDMI1	
+V3.3S	0.1A
+V5S	0.05A

HDMI2	
+V3.3S	0.1A
+V5S	0.05A

HDMI3	
+V3.3S	0.1A
+V5S	0.05A

LVDS/eDP	
+V12S	3A
+V5S	2A
+V3.3S	2A

DP1	
+V3.3S	0.5A

DP2	
+V3.3S	0.5A

DP3	
+V3.3S	0.5A

VGA	
+V3.3S	0.25A

PCIE x16	
+V12S	2.1A
+V3.3S	3A
+V3.3A	0.375A

PCIE x4_1	
+V12S	2.1A
+V3.3S	3A
+V3.3A	0.375A

PCIE x4_2	
+V12S	2.1A
+V3.3S	3A
+V3.3A	0.375A

FPGA	
+V3.3S	1.5A

USB 3.2 x4	
+V5S	3.6A

USB 2.0x4	
+V5S	2A

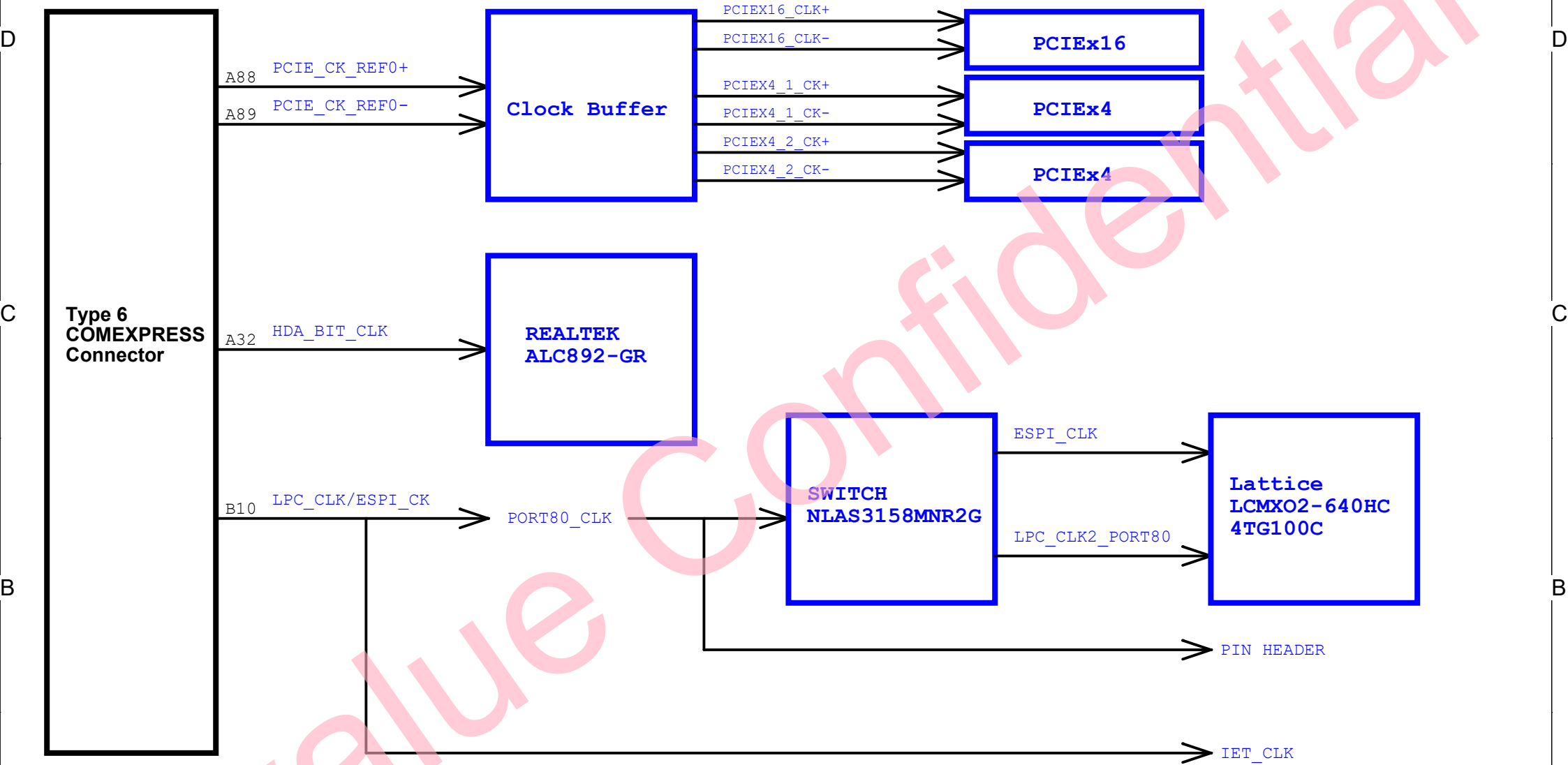
ALC892	
+V5S	0.046A
+V3.3S	0.012A

IET	
+V12S	2A
+V5S	3A

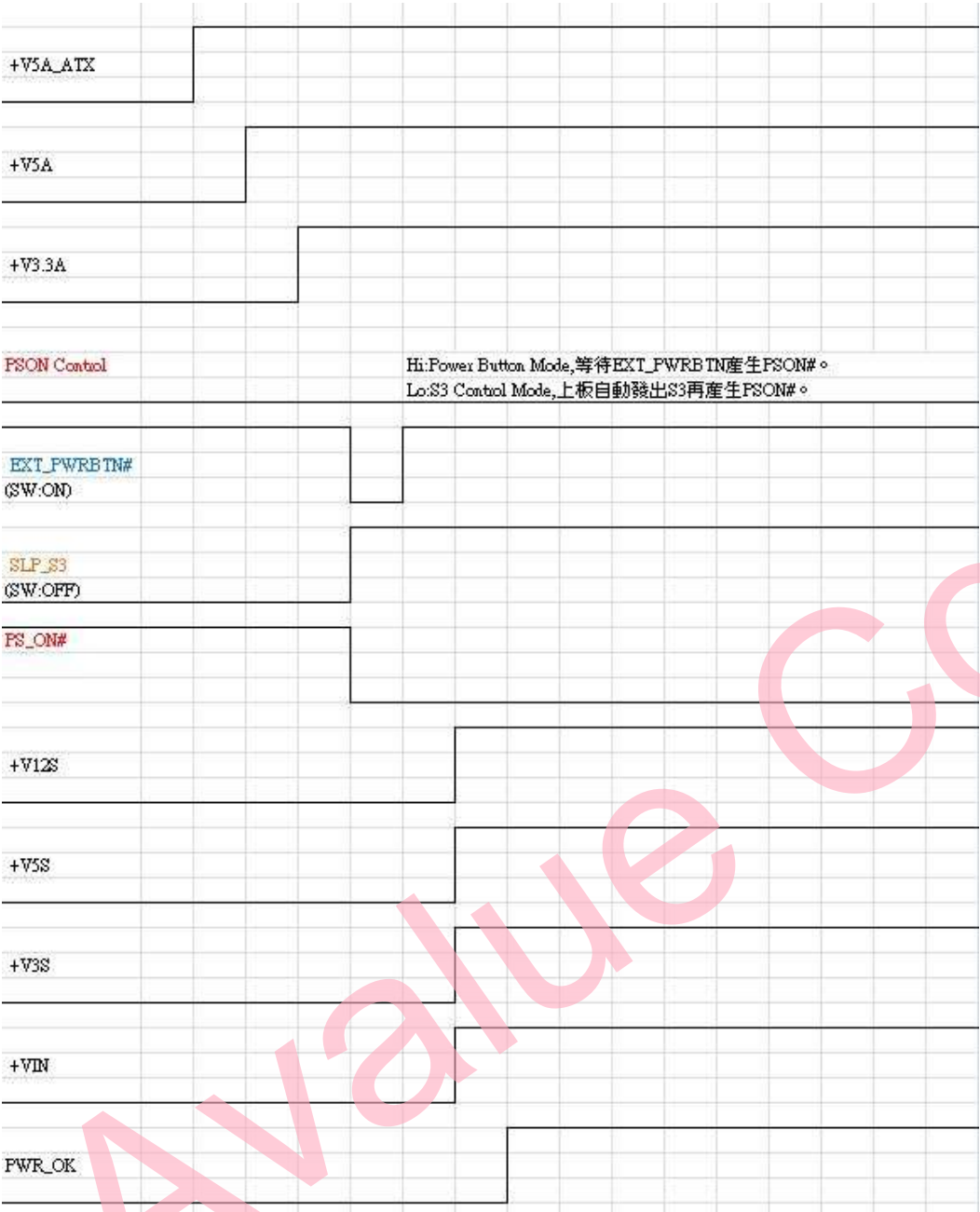
LAN	
+V3.3A	0.02A

BUZZER	
+V5S	0.044A

Clock Distribution

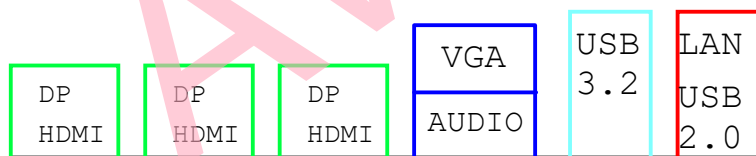
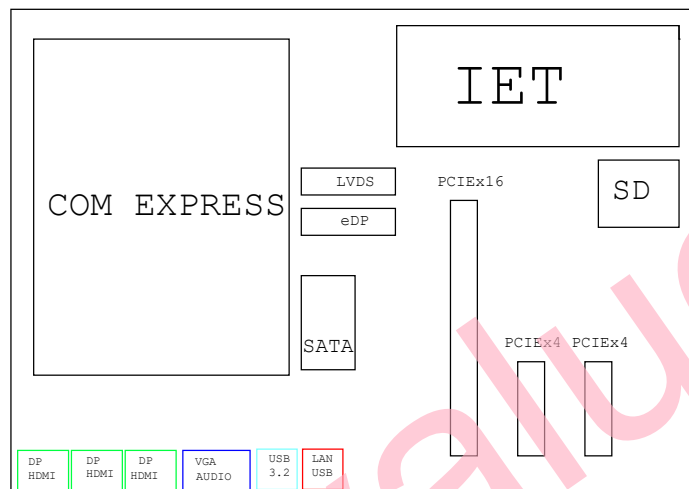


Power Sequence



Reference document

SPEC.	Com ExpressR Module Base Specification P1CMG COM.0 R3.0
Sch check list	COM Express Carrier Board Schematic Check List 20190620



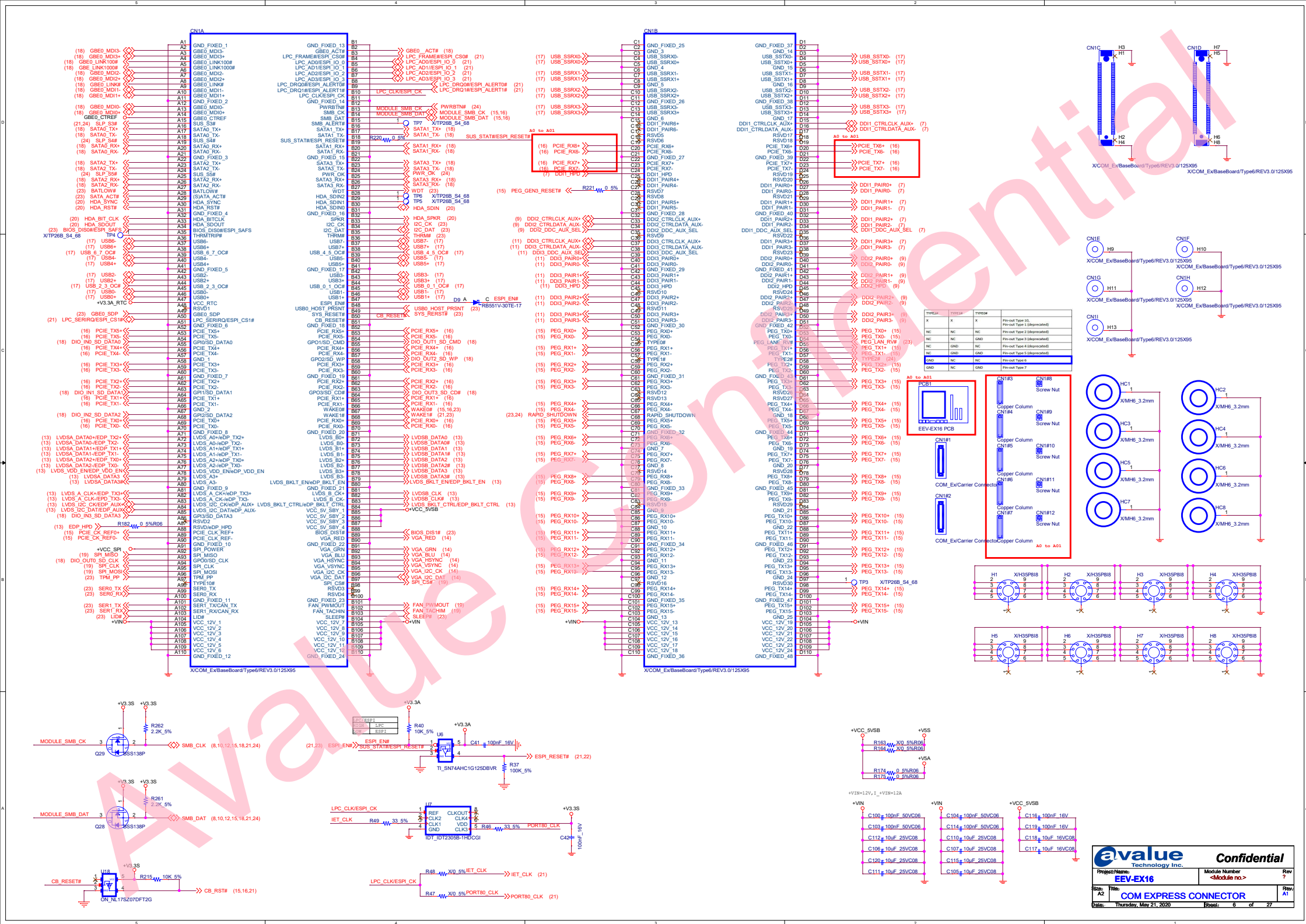
COM EXPRESS CONNECTOR

PIN(D57)	PIN(C57)	PIN(C54)	
TYPE2#	TYPE1#	TYPE0#	
X	X	X	Pin-out Type 1
NC	NC	NC	Pin-out Type 2
NC	NC	GND	Pin-out Type 3 (no IDE)
NC	GND	NC	Pin-out Type 4 (no PCI)
NC	GND	GND	Pin-out Type 5 (no IDE, no PCI)
GND	NC	NC	Pin-out Type 6 (no IDE, no PCI)

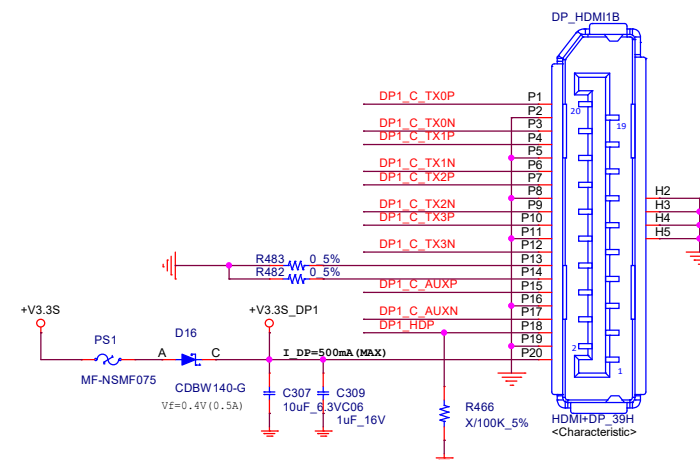
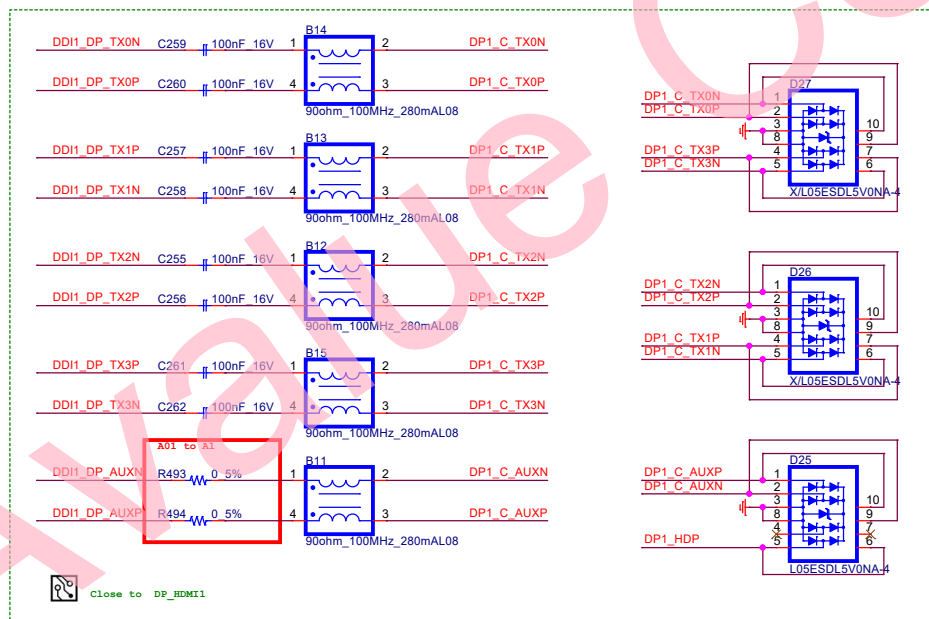
Module板對 TYPE2# 接GND ~ 以示為TYPE 6 PIN DEFINE
Carrier板用此PIN來控制12V的輸出

COM EXPRESS CONNECTOR

PIN(A97)	
TYPE10#	
NC	Pin-out R2.0
PD	Pin-out Type 10 pull down to ground with 4.7K resistor
12V	Pin-out R1.0



DP1



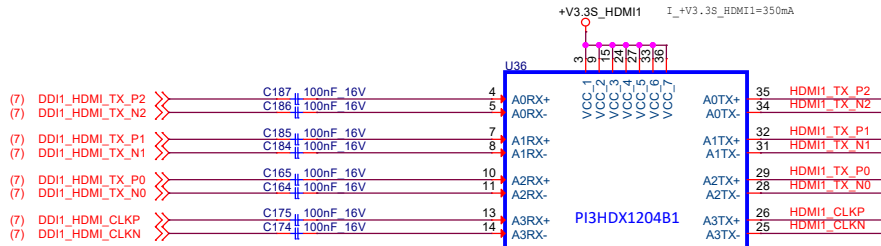


Table 3-2. Output De-emphasis Setting

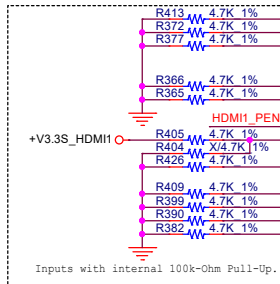
DE1	DE0	De-emphasis
0	0	0 dB
0	1	-0.5 dB
1	0	-0.7 dB
1	1	-1.0 dB

Table 3-3. Output Voltage Swing Setting

VOD1	VOD0	Output Voltage Swing
0	1	0.85 Vpp
1	1	1.15 Vpp

Table 3-4. Table 1. Signalization Setting

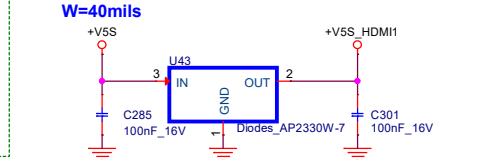
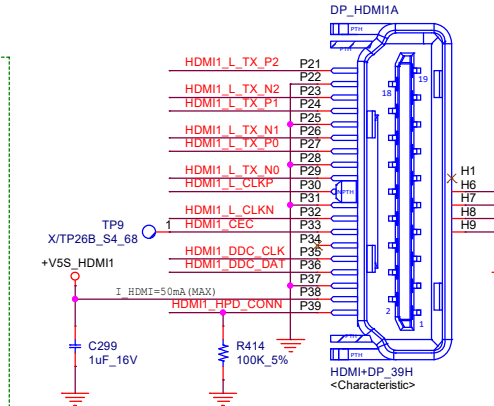
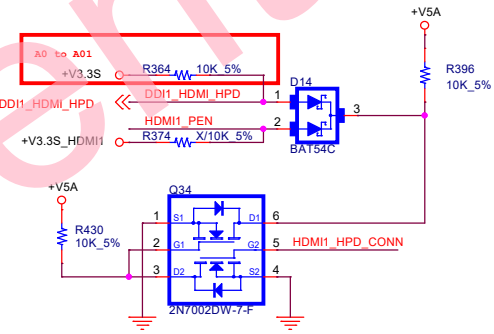
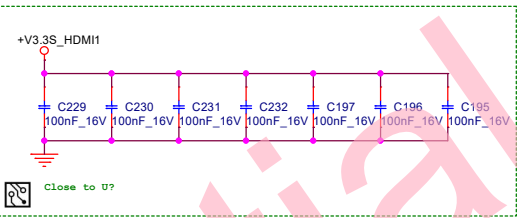
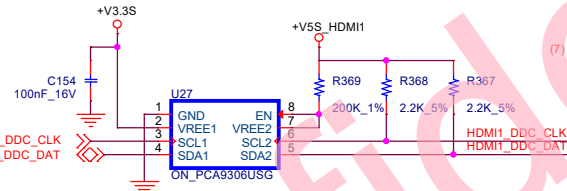
BS3	BS2	BS1	BS0	valley (VDDIO)	valley (VDDIO)
0	0	0	0	10.00	10.00
0	0	0	1	10.00	11.00
0	0	1	0	11.00	10.00
0	0	1	1	11.00	11.00
0	1	0	0	11.00	10.00
0	1	0	1	11.00	11.00
0	1	1	0	10.00	10.00
0	1	1	1	10.00	11.00
1	0	0	0	10.00	10.00
1	0	0	1	10.00	11.00
1	0	1	0	11.00	10.00
1	0	1	1	11.00	11.00
1	1	0	0	10.00	10.00
1	1	0	1	10.00	11.00
1	1	1	0	11.00	10.00
1	1	1	1	11.00	11.00



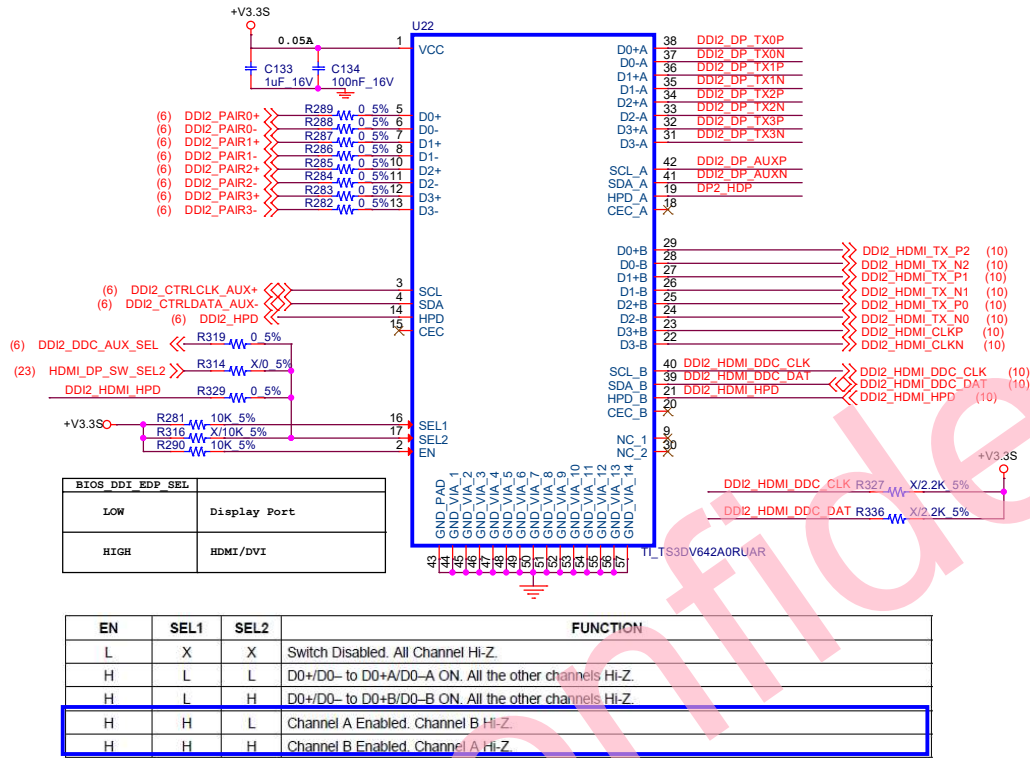
A0,1,4:
I2C programmable address bits.

PEN : Power Enable.

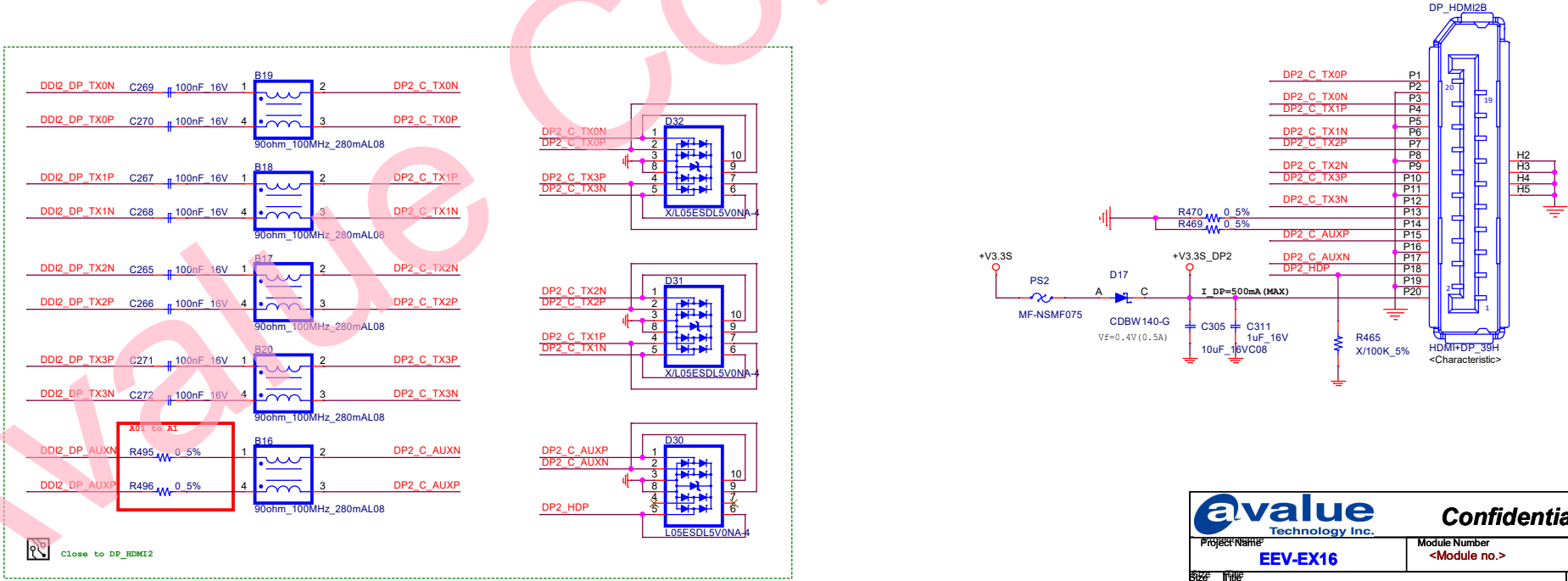
Pin Mode (ENI2C):
When HIGH, each channel is programmed
by the external pin voltage.
When LOW, each channel is programmed
by the data stored in the I2C bus.

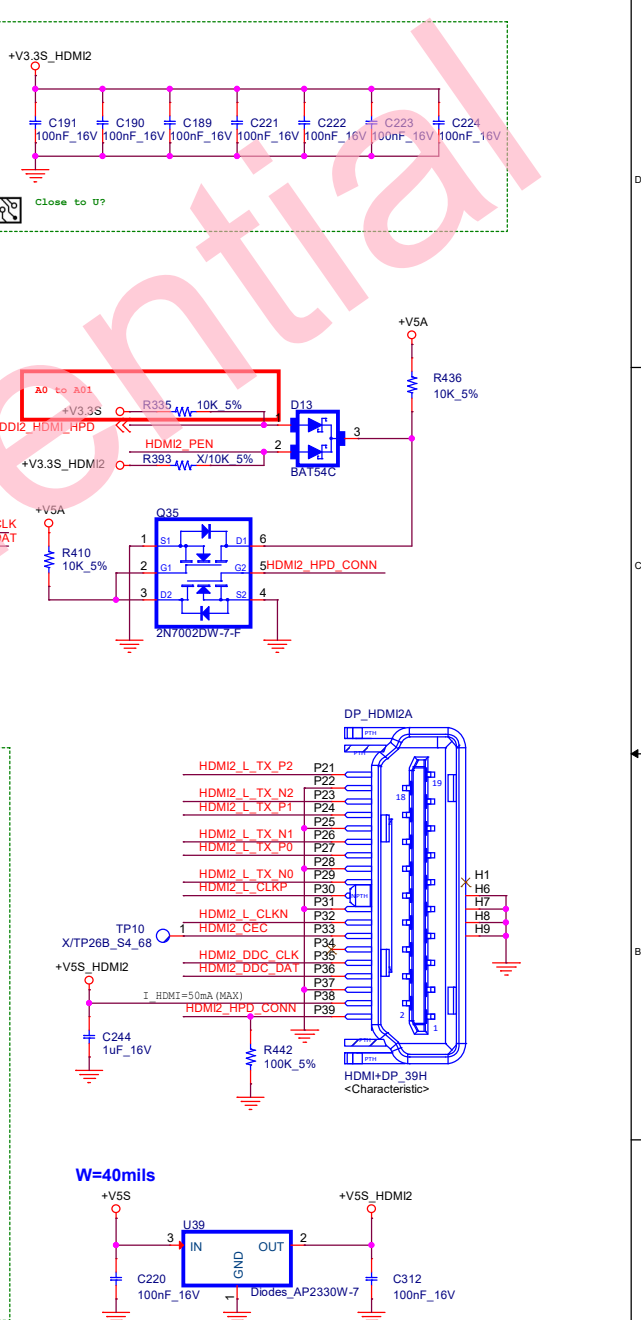
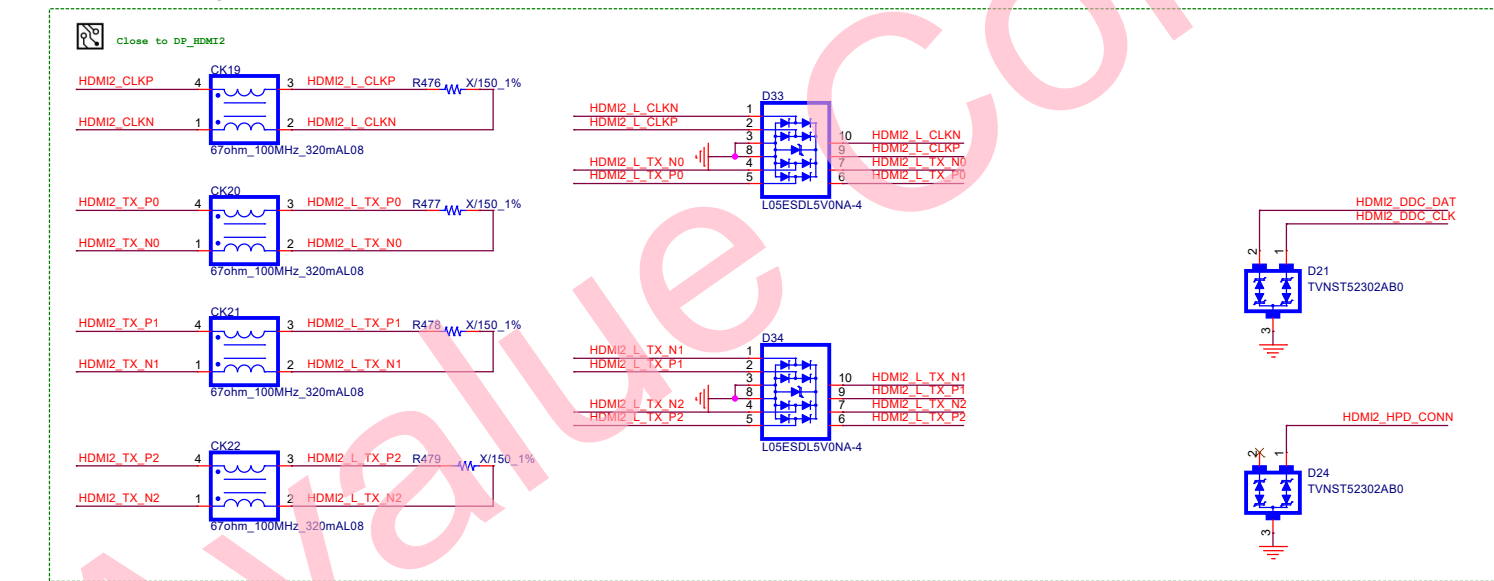
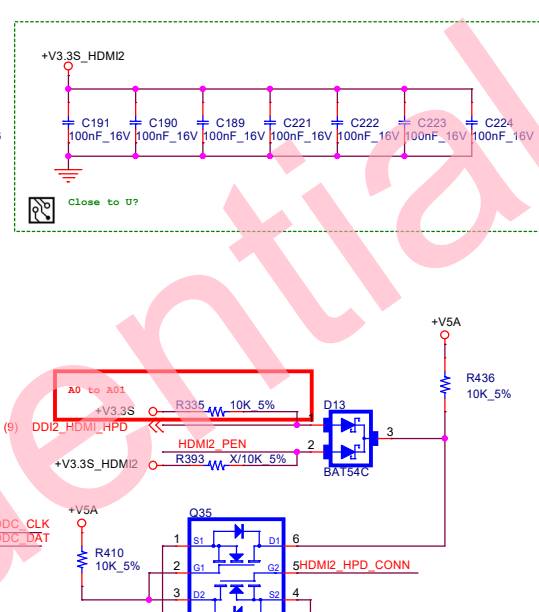
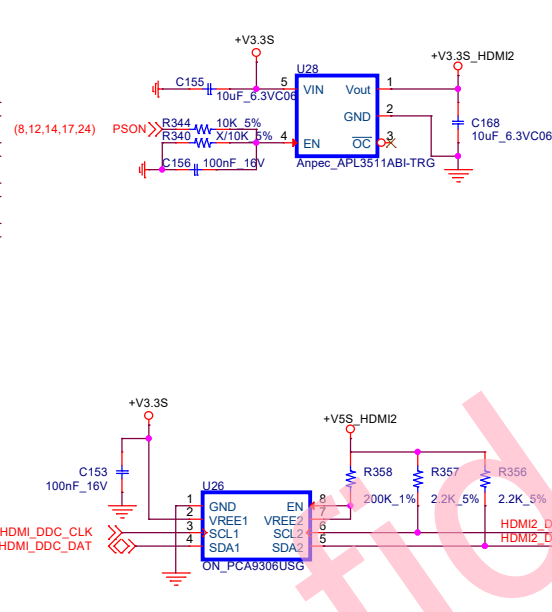
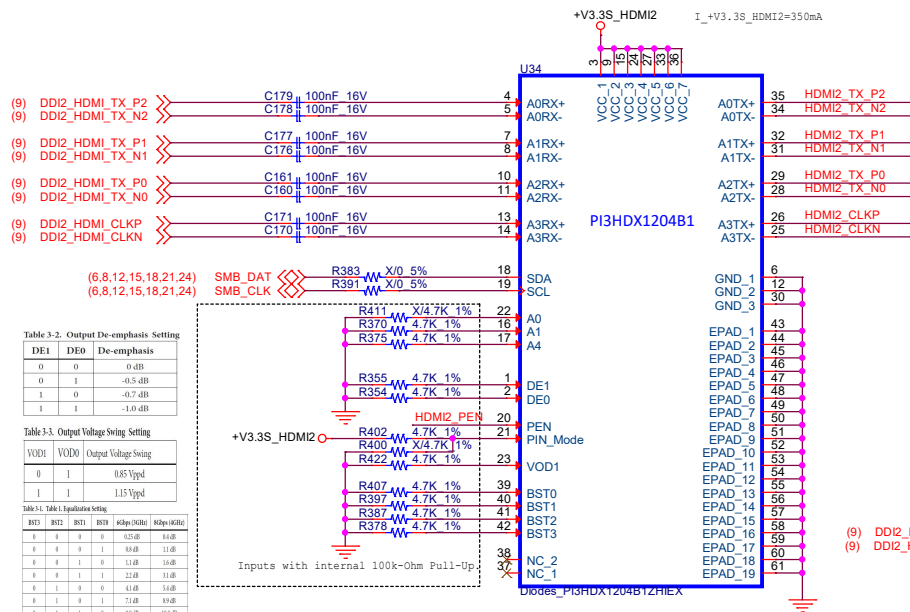


DDI2 switch

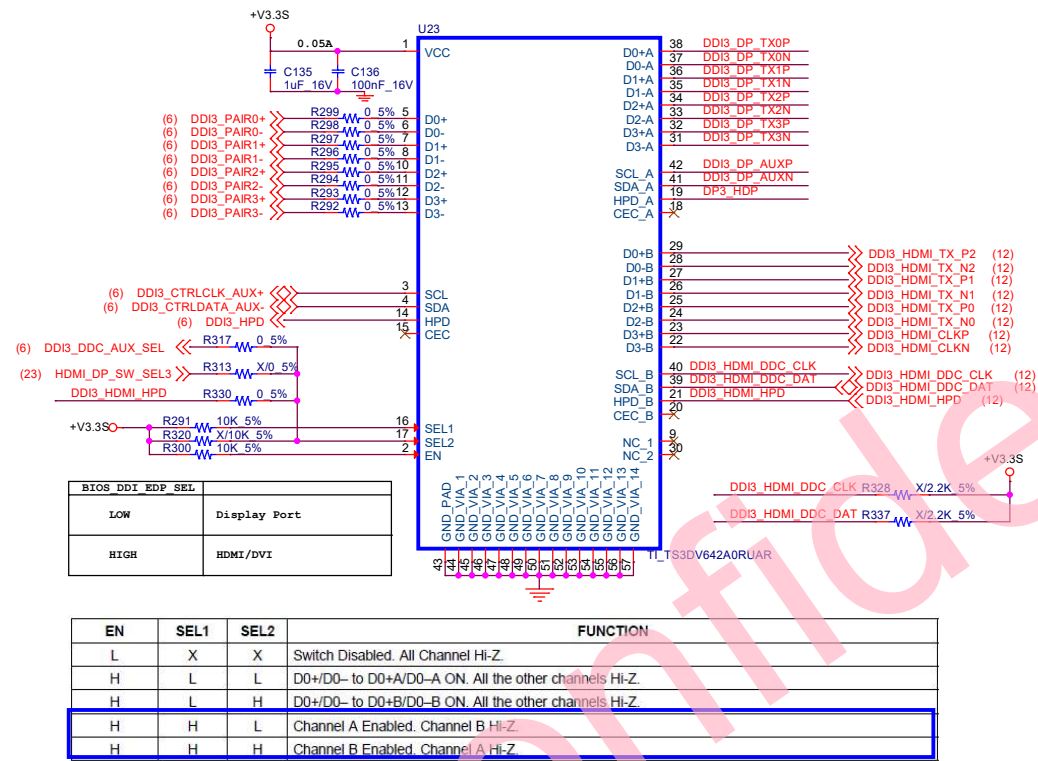


DP2

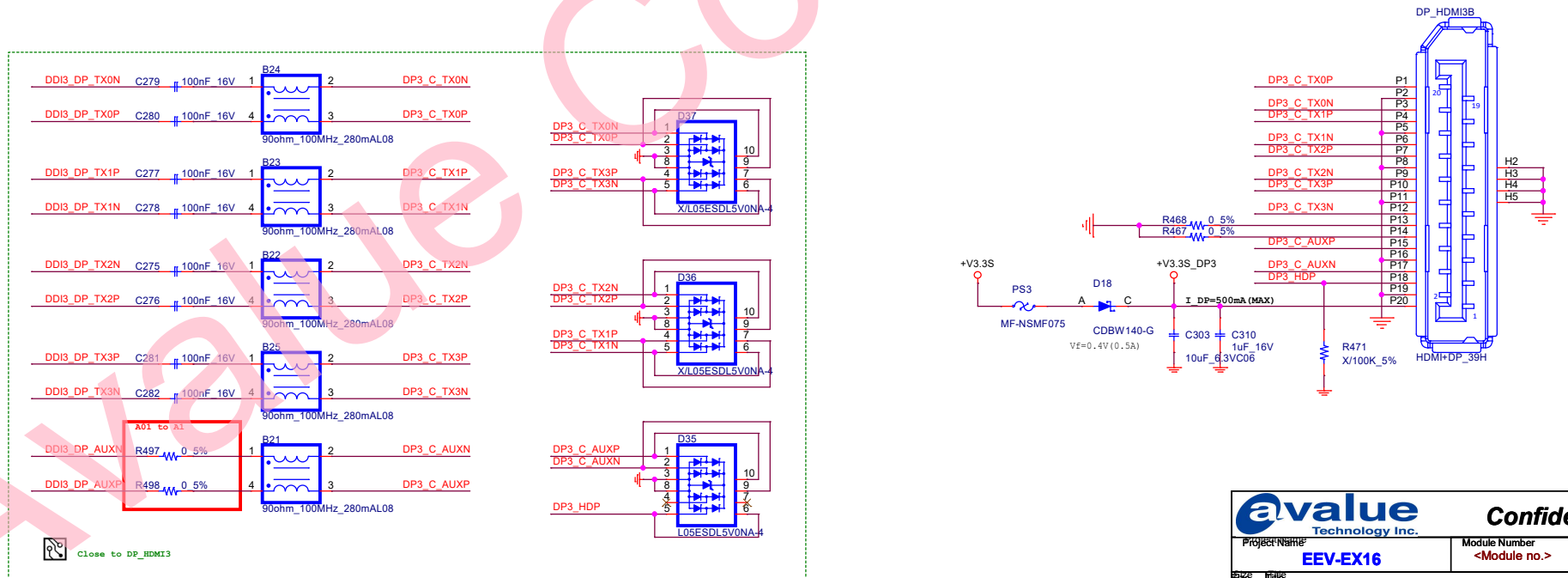




DDI3 switch



DP3



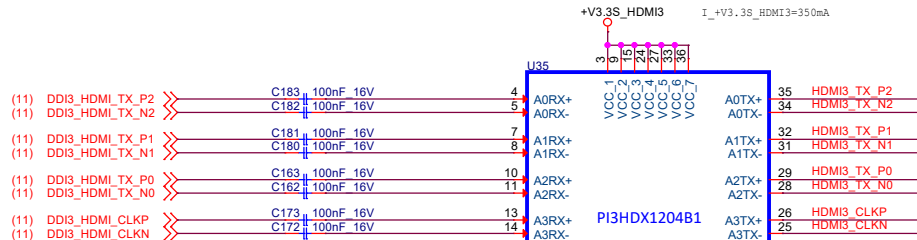


Table 3-3. Output Voltage Swing Setting

VOD1	VOD0	Output Voltage Swing
0	1	0.85 Vpp
1	1	1.15 Vpp

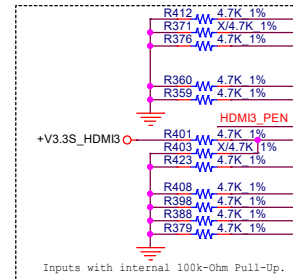
Table 3-2. Output De-emphasis Setting

DE1	DE0	De-emphasis
0	0	0 dB
0	1	-0.5 dB
1	0	-0.7 dB
1	1	-1.0 dB

Table 3-1. I2C Register Setting

BS3	BS2	BS1	BS0	Value (Hex)	Value (Dec)
0	0	0	0	0x00	0
0	0	0	1	0x01	1
0	0	1	0	0x02	2
0	0	1	1	0x03	3
0	1	0	0	0x04	4
0	1	0	1	0x05	5
0	1	1	0	0x06	6
0	1	1	1	0x07	7
1	0	0	0	0x08	8
1	0	0	1	0x09	9
1	0	1	0	0x0A	10
1	0	1	1	0x0B	11
1	1	0	0	0x0C	12
1	1	0	1	0x0D	13
1	1	1	0	0x0E	14
1	1	1	1	0x0F	15

(6,8,10,15,18,21,24)
(6,8,10,15,18,21,24)



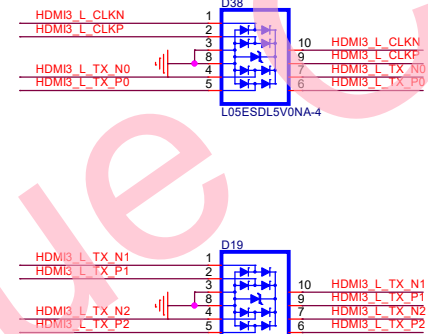
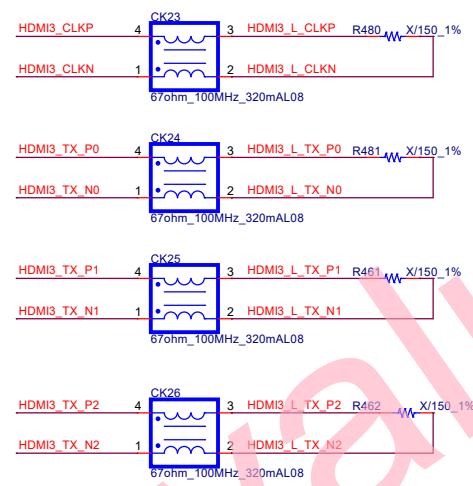
A0,1,4:
I2C programmable address bits.

PEN : Power Enable.

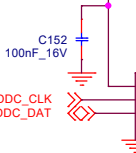
Pin_Mode (ENI2C):
When HIGH, each channel is programmed
by the external pin voltage.

When LOW, each channel is programmed
by the data stored in the I2C bus.

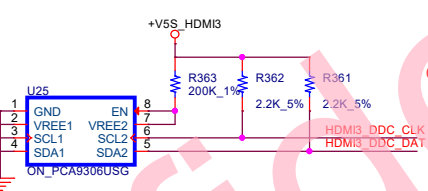
Close to JDP_HDMI1B



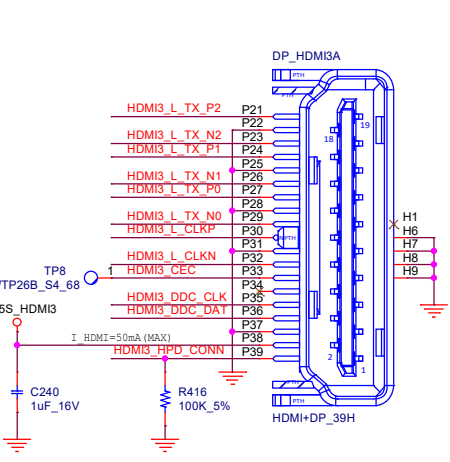
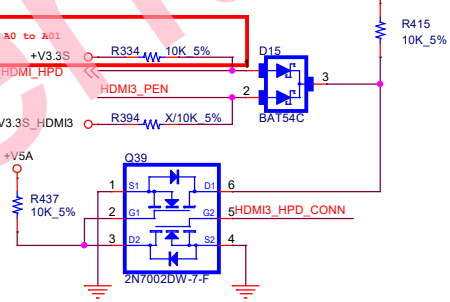
(8,10,14,17,24)



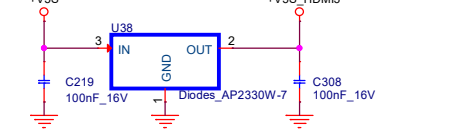
(11) DDI3_HDMI_DDC_CLK
(11) DDI3_HDMI_DDC_DAT



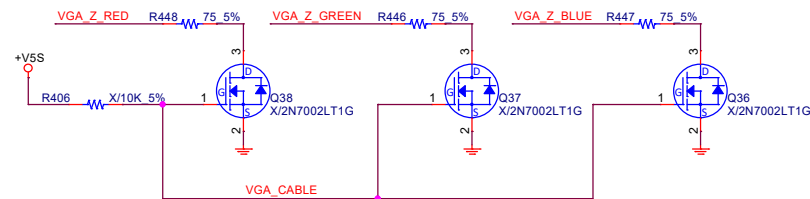
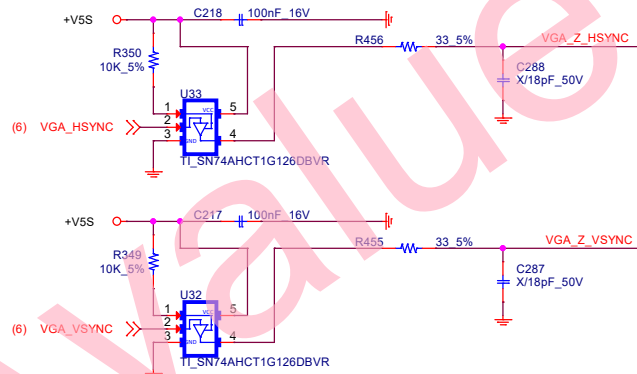
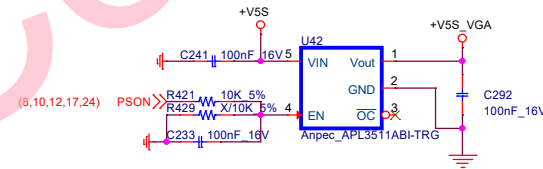
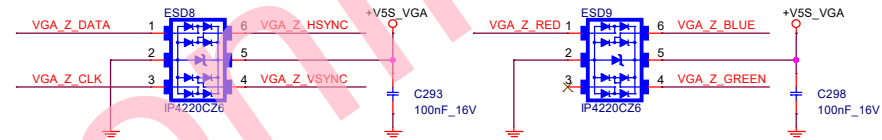
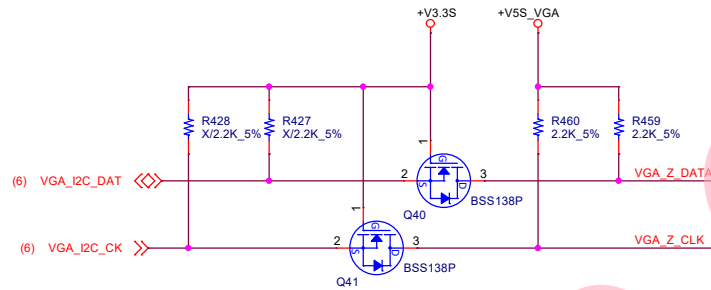
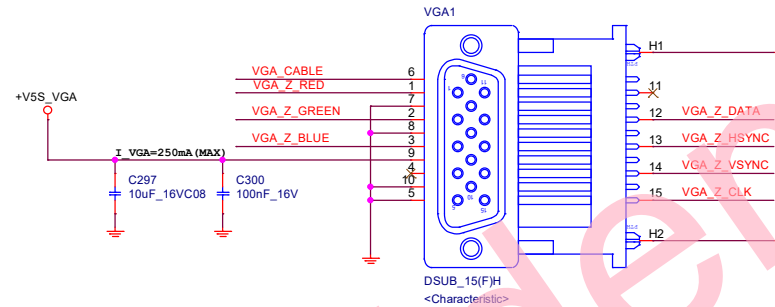
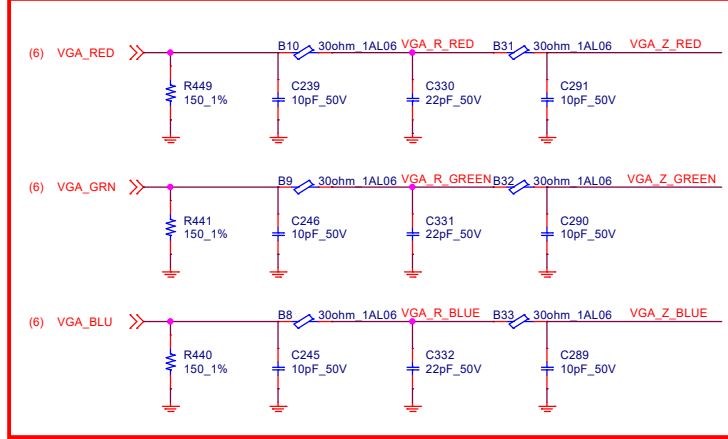
(11) DDI3_HDMI_HPD

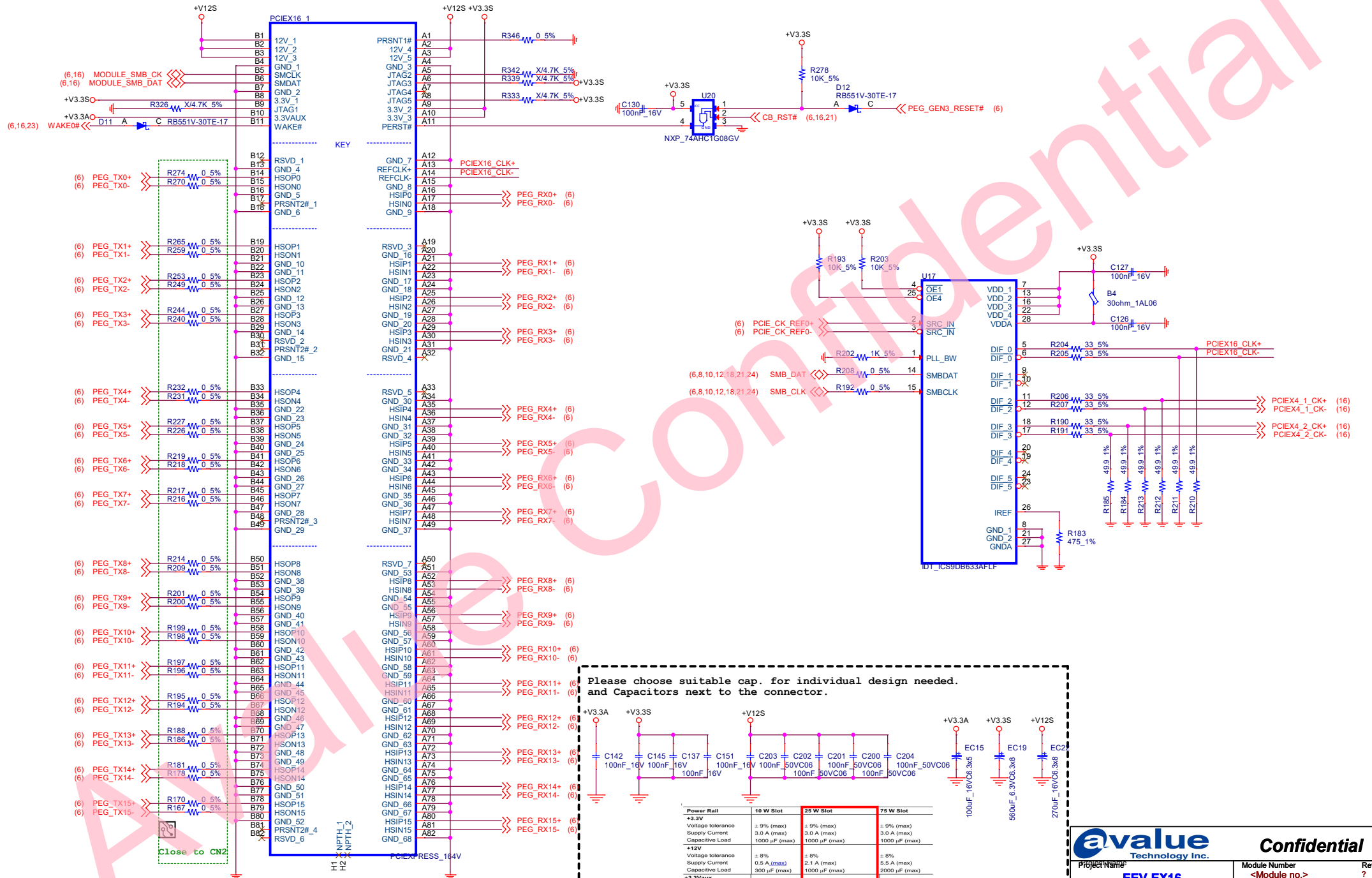


W=40mils



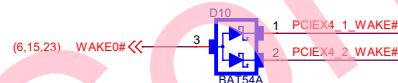
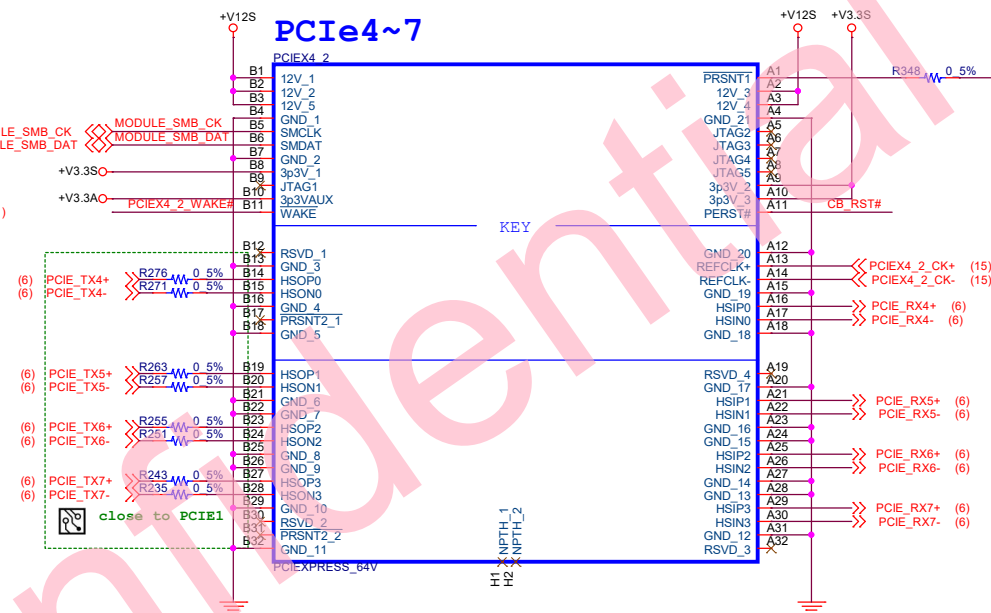
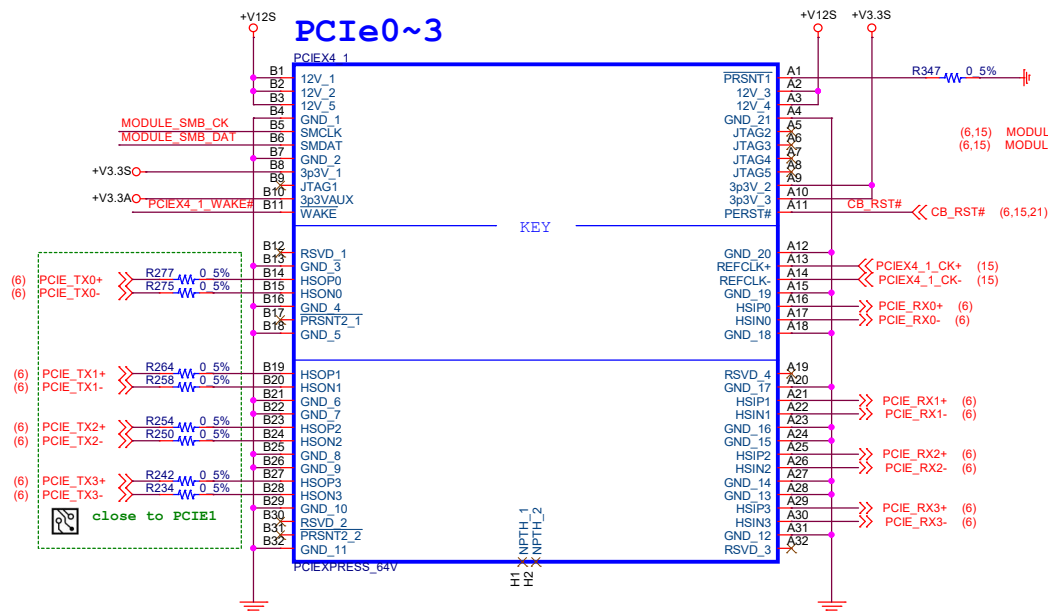
A0 to A01



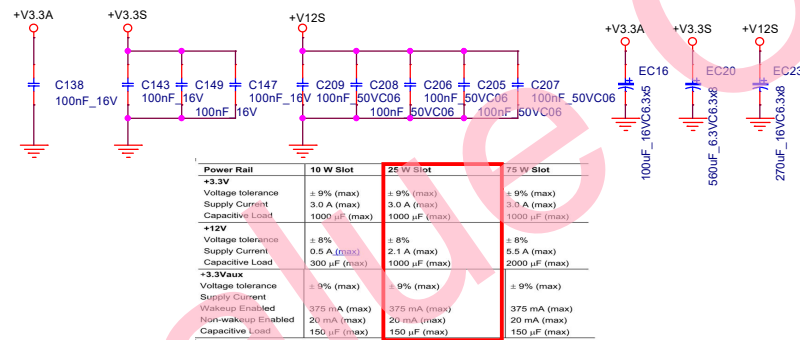


Please choose suitable cap. for individual design needed.
and Capacitors next to the connector.

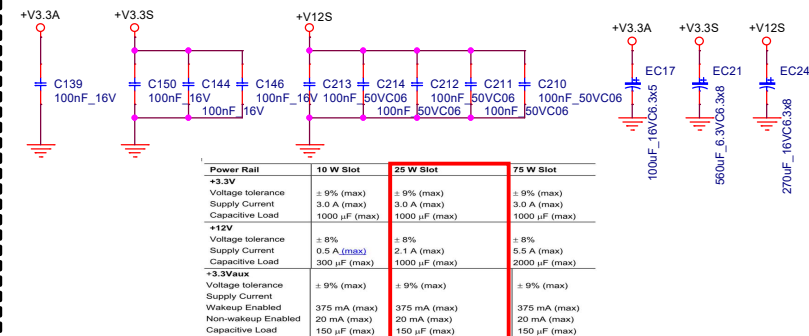
Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3V			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)	1000 µF (max)
+12V			
Voltage tolerance	± 8%	± 8%	± 8%
Supply Current	0.5 A (max)	2.1 A (max)	0.5 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	2000 µF (max)
+3.3Vaux			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	375 mA (max)	375 mA (max)	375 mA (max)
Wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Non-wakeup Enabled	150 µF (max)	150 µF (max)	150 µF (max)
Capacitive Load	150 µF (max)	150 µF (max)	150 µF (max)



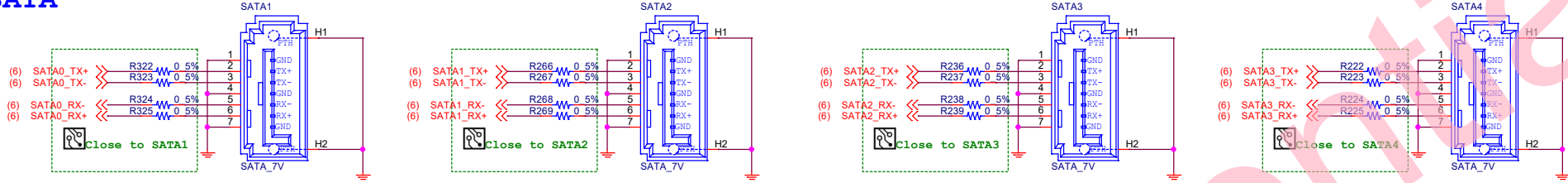
Please choose suitable cap. for individual design needed.
and Capacitors next to the connector.



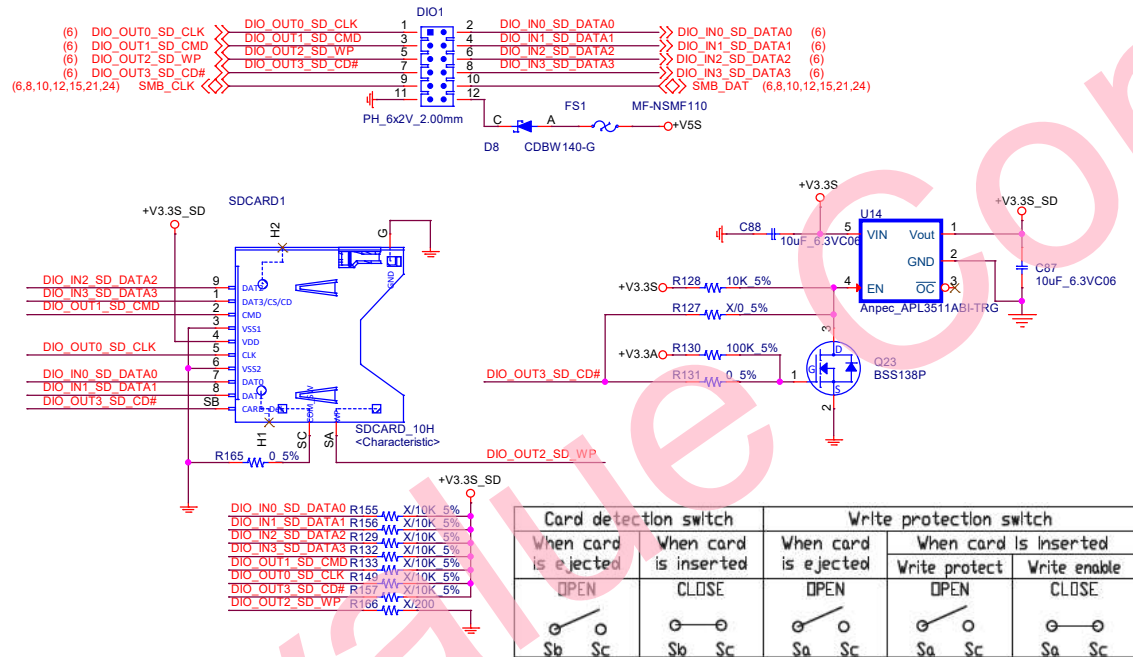
Please choose suitable cap. for individual design needed.
and Capacitors next to the connector.



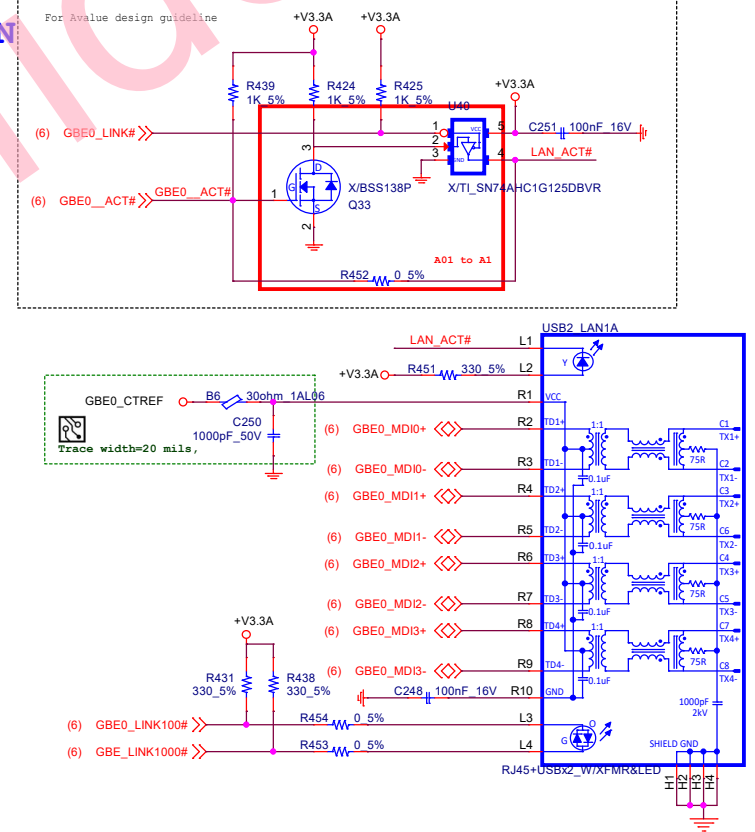
SATA



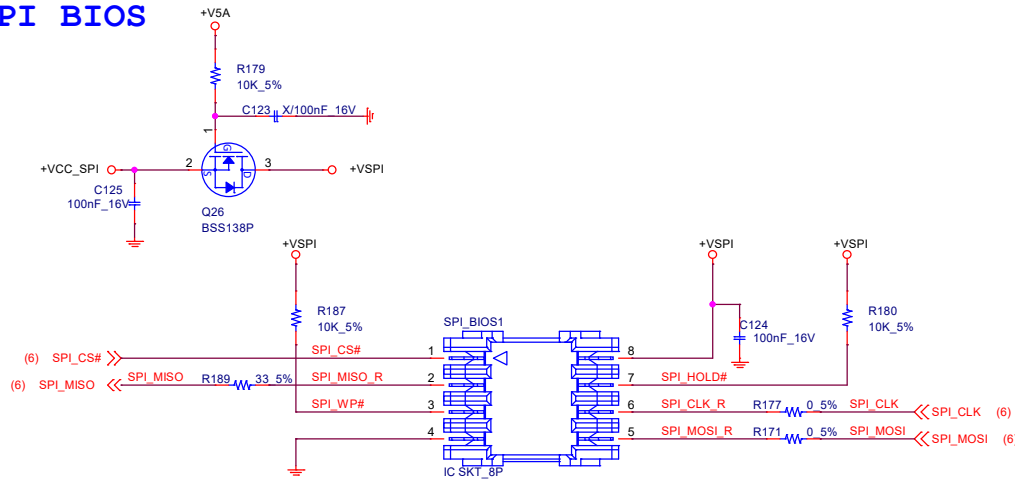
DIO/SDIO



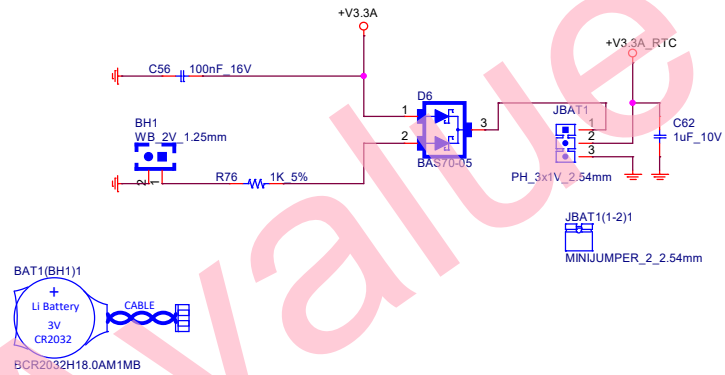
LAN



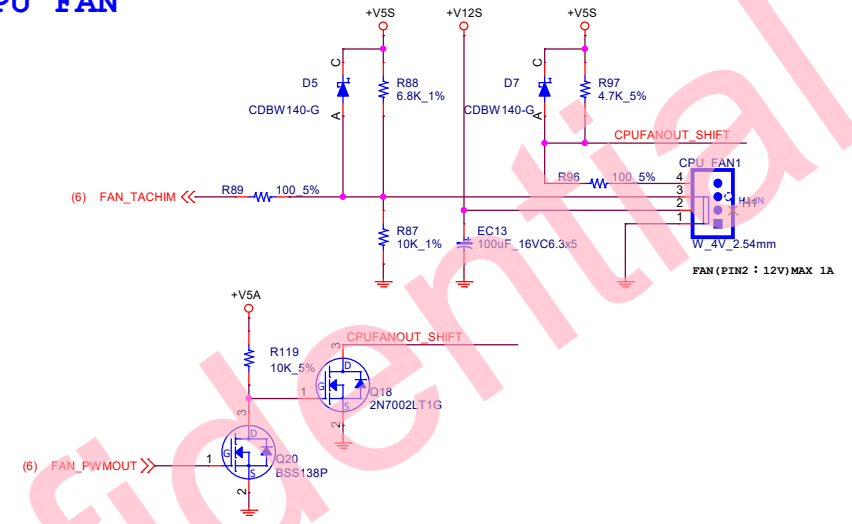
SPI BIOS



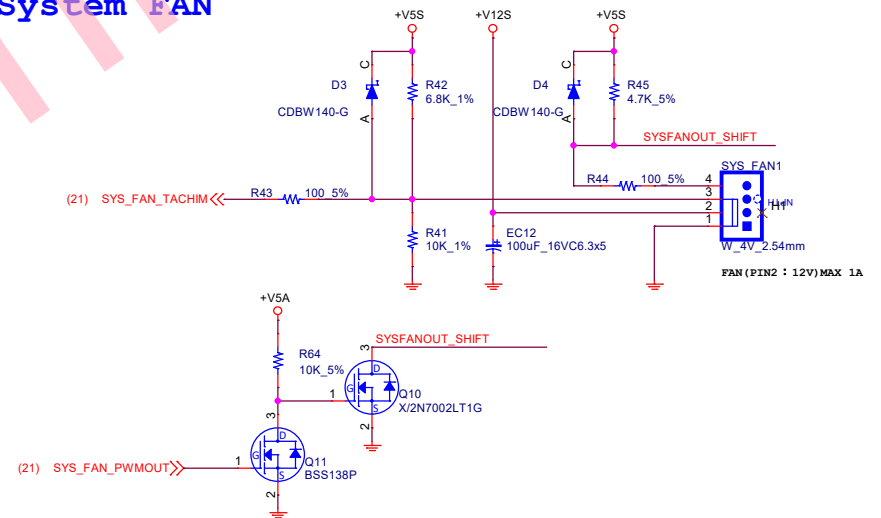
RTC BATTERY

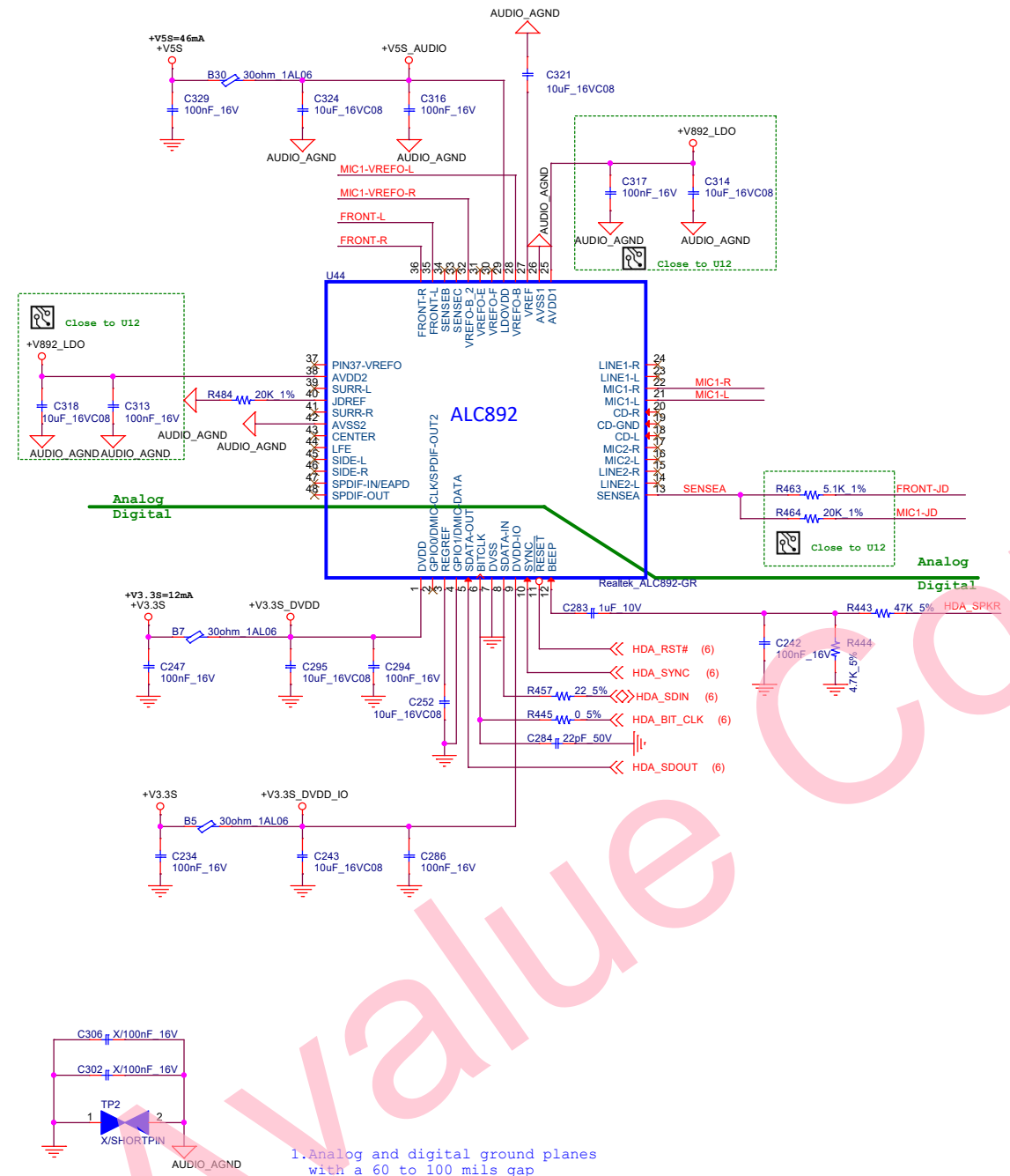


CPU FAN



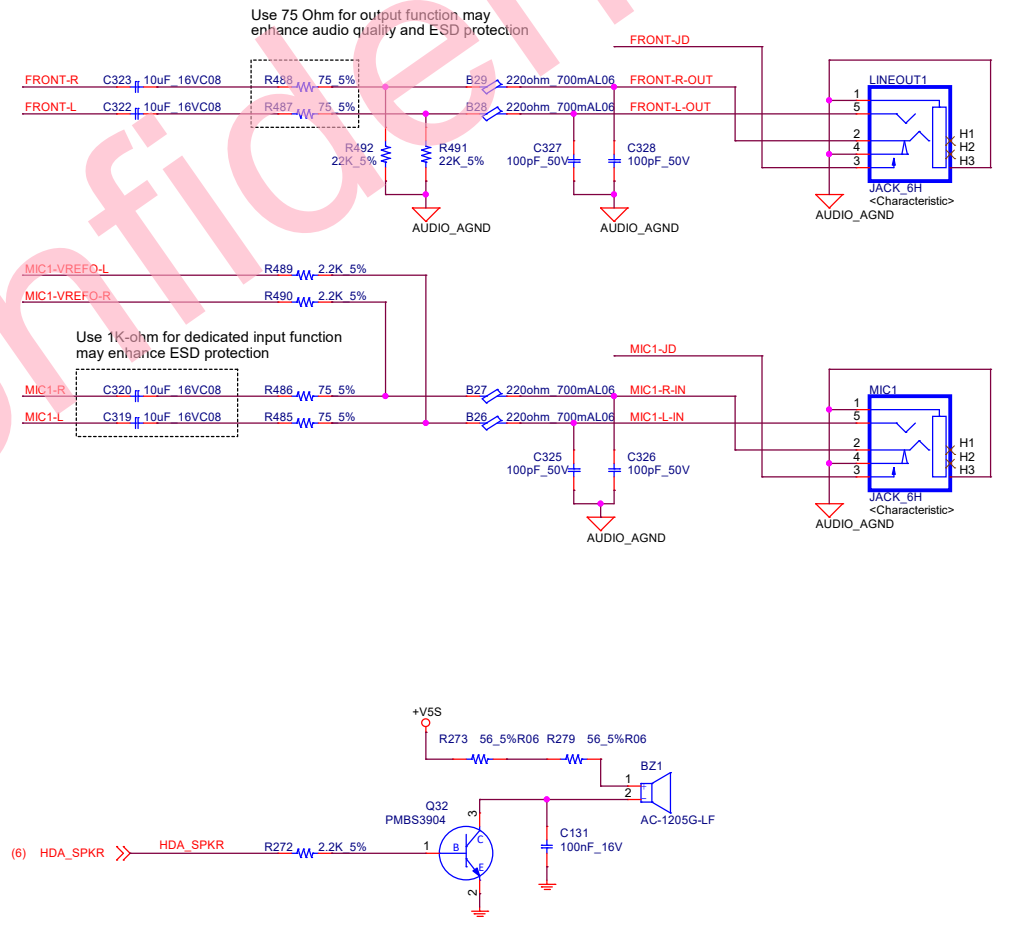
System FAN



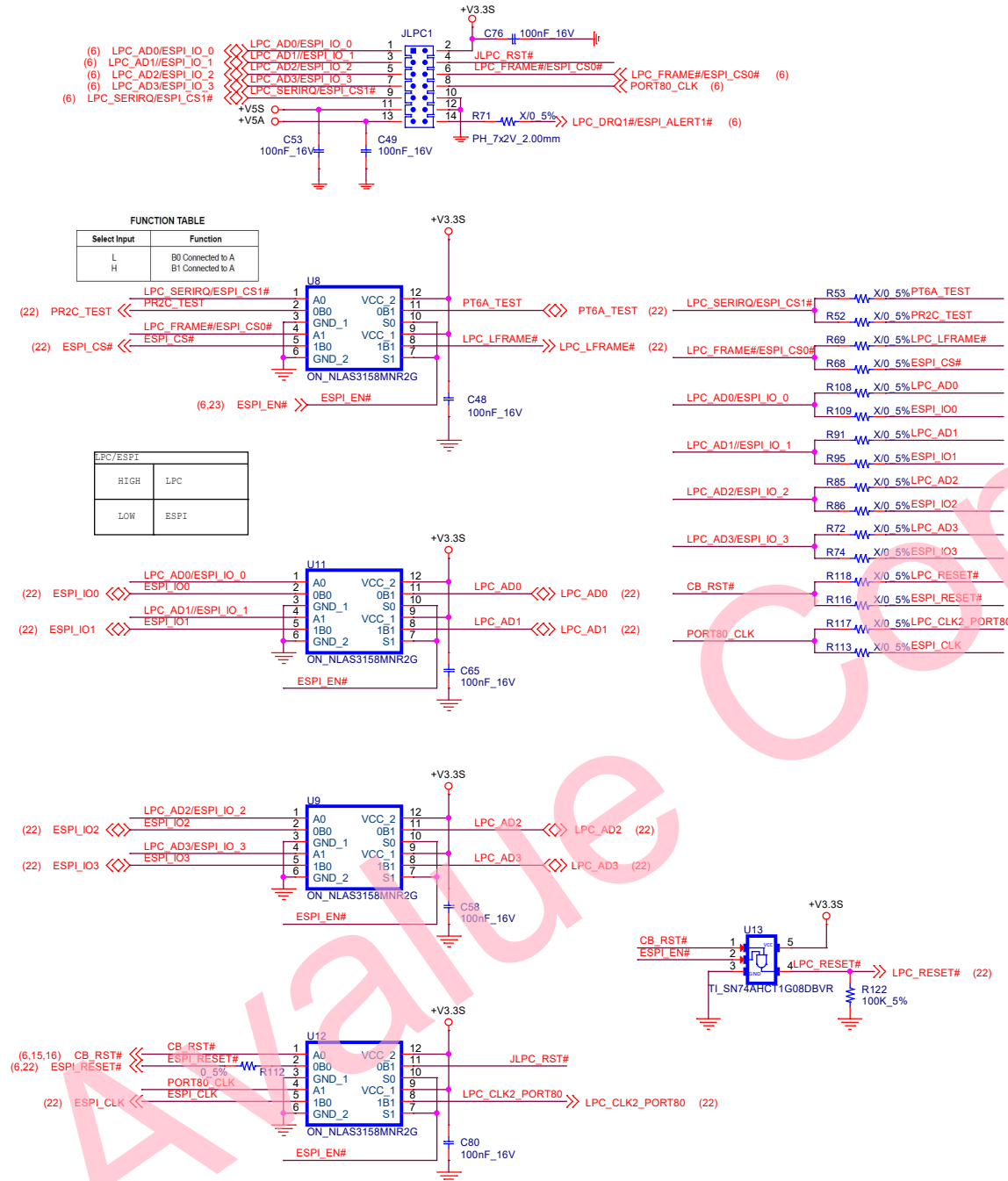


Tied at one point only under the codec or near the codec

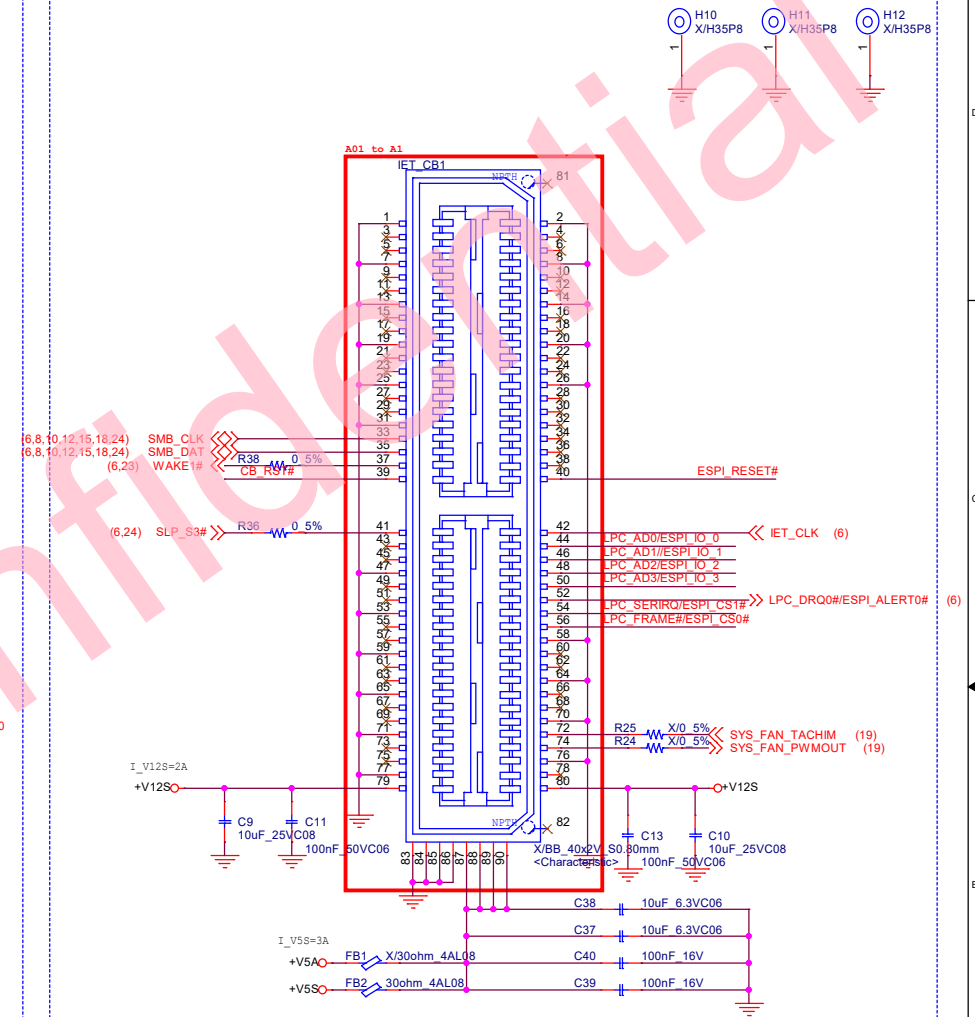
1. Analog and digital ground planes with a 60 to 100 mils gap
2. The digital and analog ground planes are tied together by a wide link, about 50mils

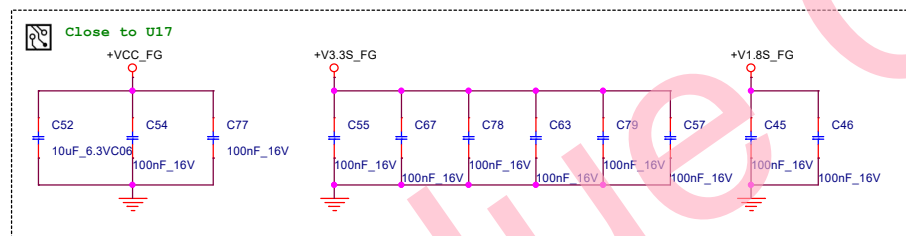
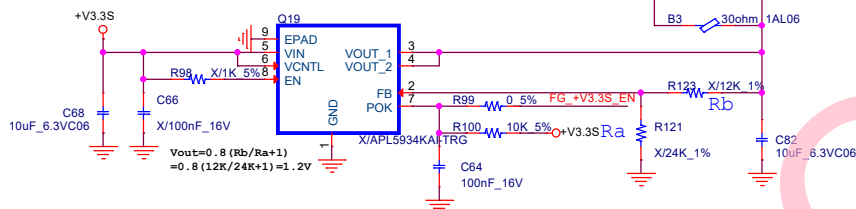
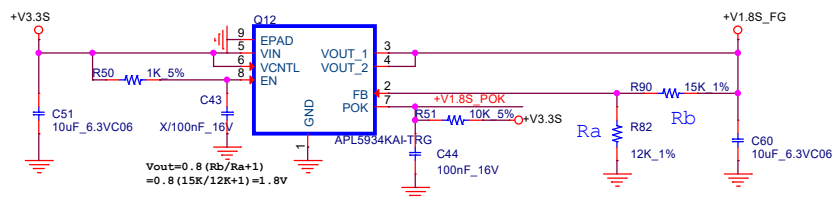
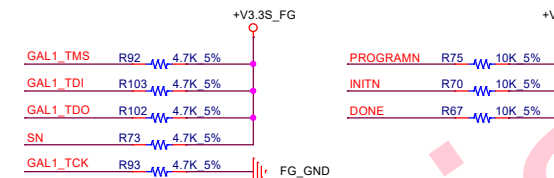
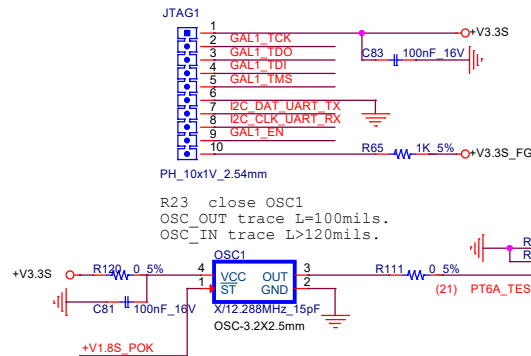
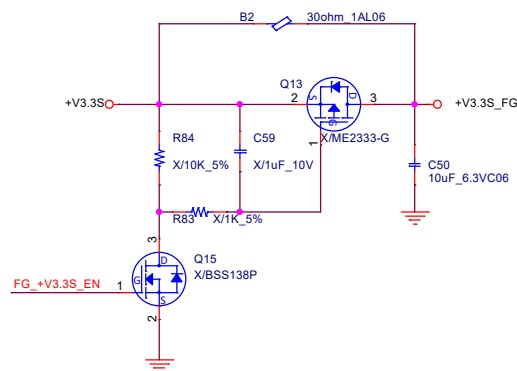


PORT 80

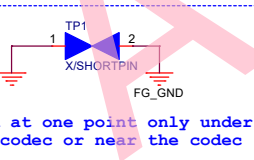
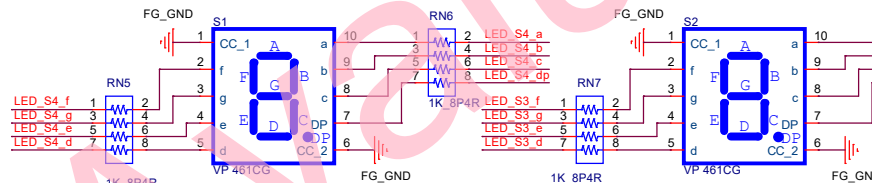


IET

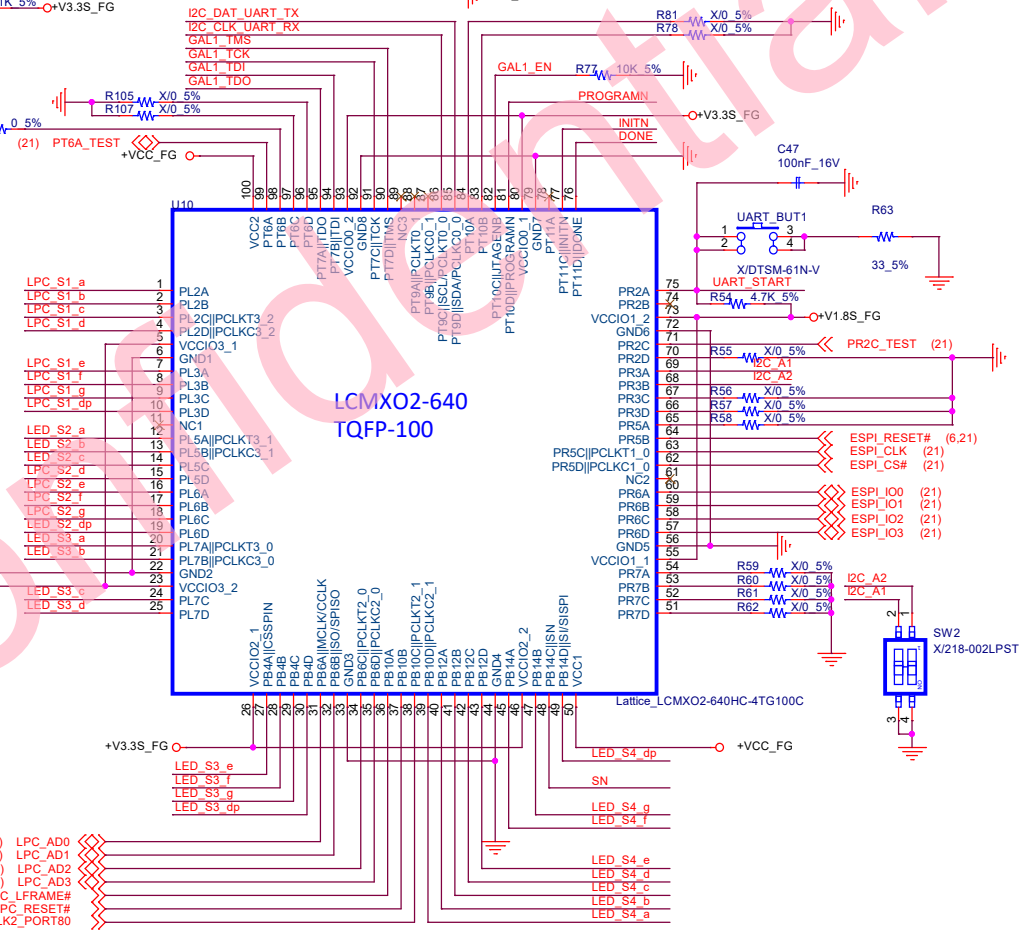
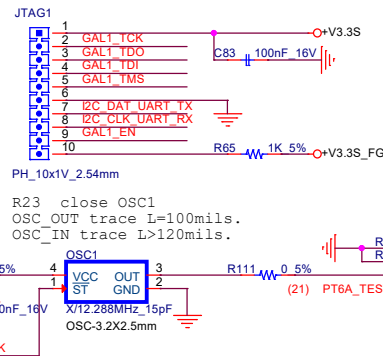




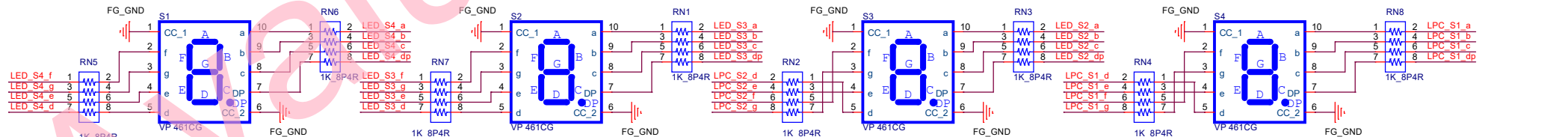
MSB



1. Analog and digital ground planes with a 60 to 100 mils gap
2. The digital and analog ground planes are tied together by a wide link, about 50mils



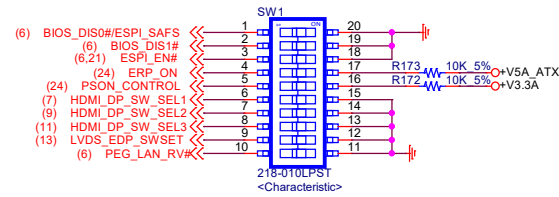
LSB



		Confidential	
Project Name EEV-EX16		Module Number <Module no.>	
Size A3		Title FPGA	
Date: Thursday, May 21, 2020		Sheet 22 of 27	

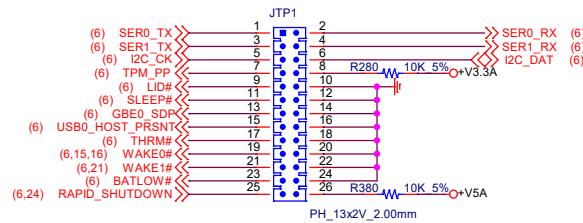
SW1 Setting

	Function	OFF	ON
1	BIOS ROM select	Default	
2	BIOS ROM select	Default	
3	LPC/eSPI select	LPC	eSPI
4	ERP setting	ERP OFF	ERP ON
5	PSON control	S3	Power button
6	DP/HDMI select1 (optional)	HDMI1	DP1
7	DP/HDMI select2 (optional)	HDMI2	DP2
8	DP/HDMI select3 (optional)	HDMI3	DP3
9	LVDB/eDP select (optional)	eDP	LVDB
10	PCIeX16 reverse select	Normal	Reverse



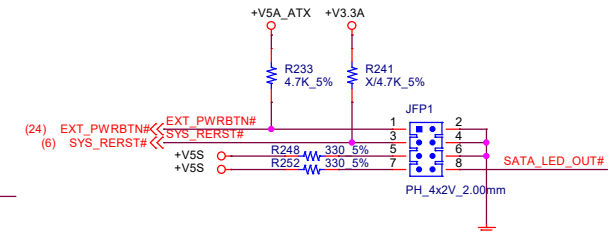
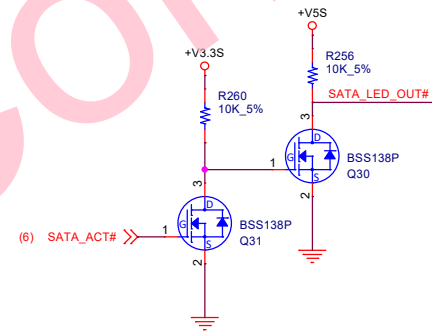
ESPI_EN#	BIOS_DIS#	BIOS_DIS#	Boot Bus	BBS	Chipset ESPI_CS# Destination	Carrier ESPI_CS# Pin	Chipset SPI_CS# Destination	Chipset SPI_CS# Destination	Carrier SPI_CS# Pin	SPI Descriptor	Ref to Images Above	Notes
1	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	A	MAFS on Module LPC bus enabled
1	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	B	MAFS on Carrier LPC bus enabled
1	1	0	-	0	-	-	-	-	High	-	-	Not used - was FWV
1	1	1	SPI	0	-	-	Module	Module	High	Module	A	MAFS on Module LPC bus enabled
0	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	C	MAFS on Module ESPI bus enabled
0	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	D	MAFS on Carrier ESPI bus enabled
0	1	0	eSPI	1	Module	-	-	-	SPI0	Module	E	SAFS and BMC on Module ESPI bus enabled
0	1	1	eSPI	1	Carrier	Chipset ESPI_CS#	-	-	SPI0	Carrier	F	SAFS and BMC on Carrier ESPI bus enabled

Test position



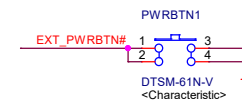
Function	Pin define
Serial port0	1 SER0_TX 2 SER0_RX
Serial port1	3 SER1_TX 4 SER1_RX
I2C	5 I2C_CK 6 I2C_DAT
TPM_PP	7 TPM_PP 8 +V3.3A
LID switch	9 LID# 10 GND
Sleep button	11 SLEEP# 12 GND
IEEE 1588 SDP	13 GBE0_SDP 14 GND
USB0_HOST_PRNT	15 USB0_HOST_PRNT 16 GND
Over-temp	17 THRM# 18 GND
PCI Express wake up	19 WAKE0# 20 GND
General wake up	21 WAKE1# 22 GND
Battery low	23 BATLOW# 24 GND
Rapid Shutdown	25 RAPID_SHUTDOWN 26 +V5A

Front panel

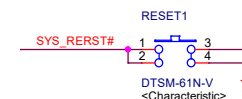


Function	Pin define
Power button	1 PWRBTN# 2 GND
Reset button	3 RERST# 4 GND
Power LED	5 +V5S 6 GND
SATA LED	7 +V5S 8 SATA_LED#

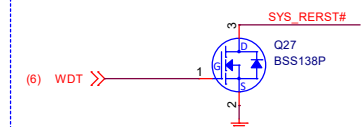
Power button



Reset button

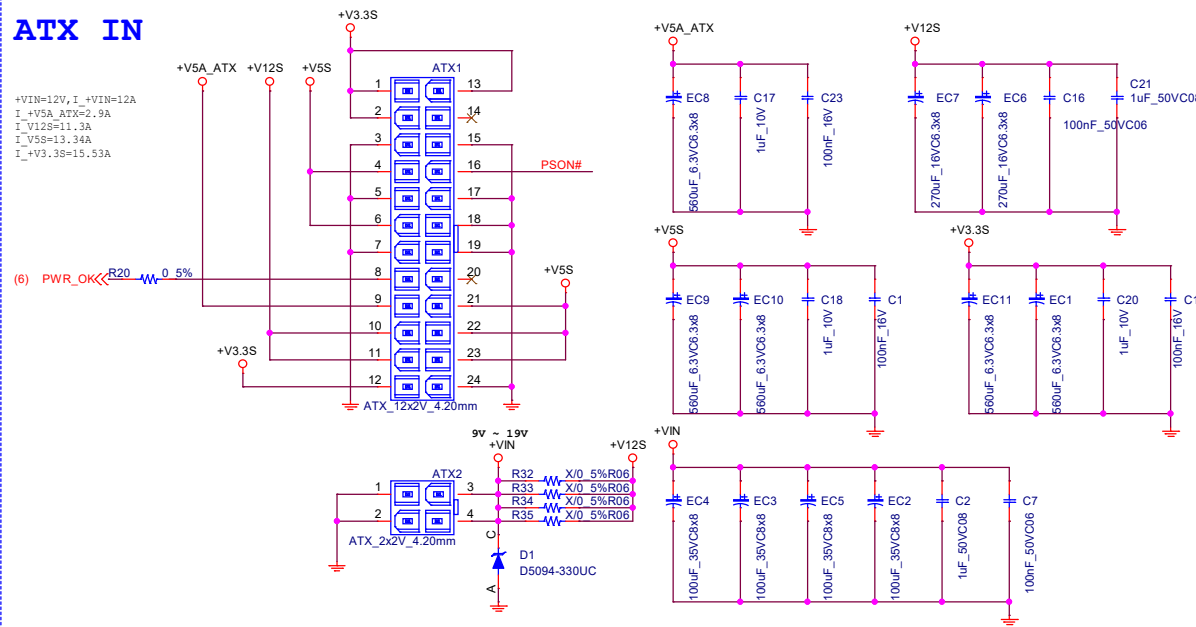


WDT

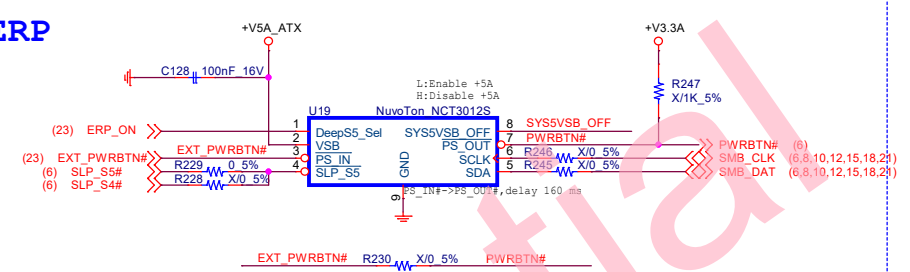


ATX IN

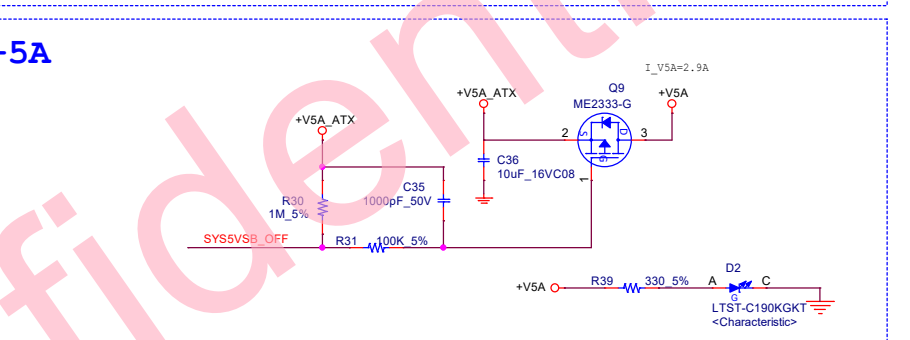
+VIN=12V, I_{VIN}=12A
I_{+V5A_ATX}=2.9A
I_{+V12S}=1.3A
I_{+V5S}=13.34A
I_{+V3.3S}=15.53A



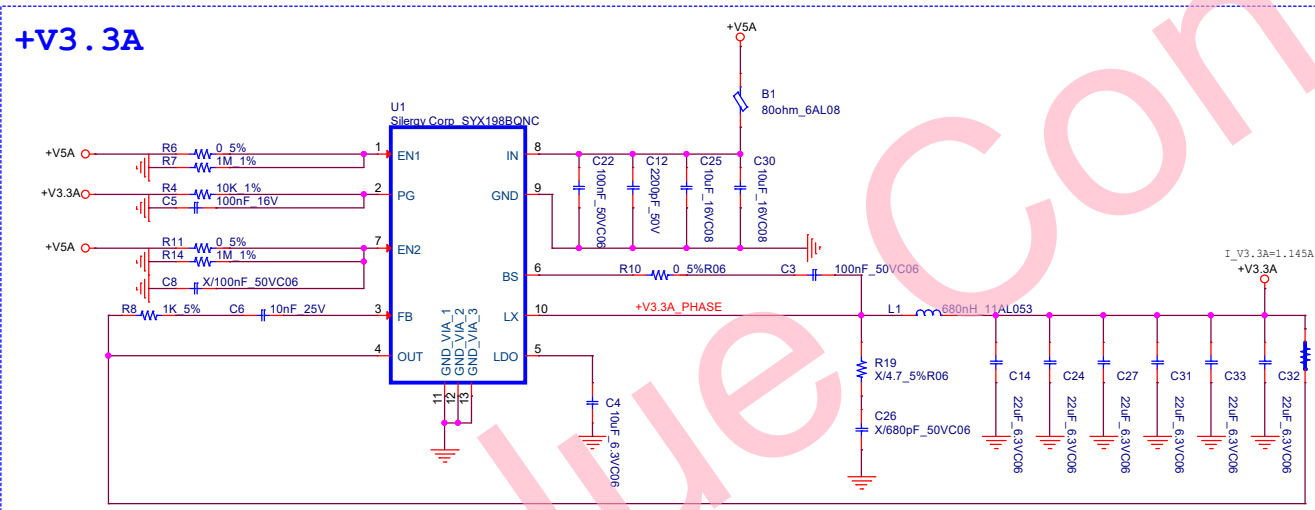
ERP



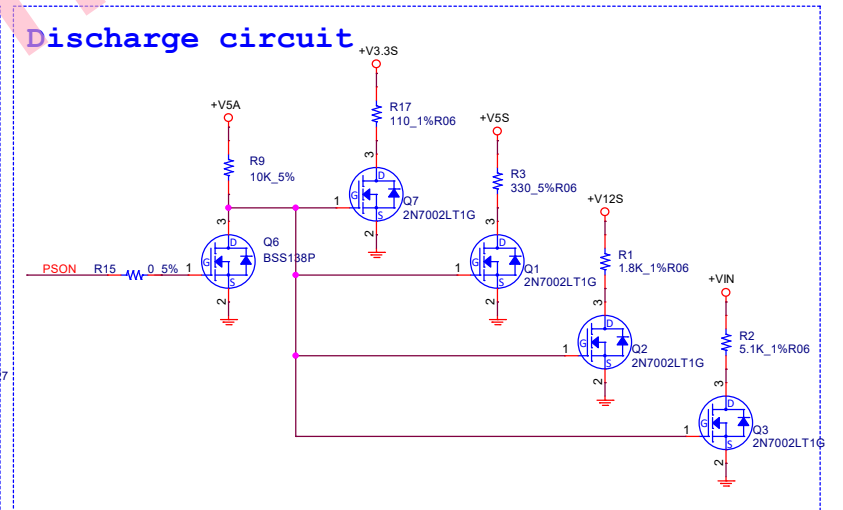
+5A



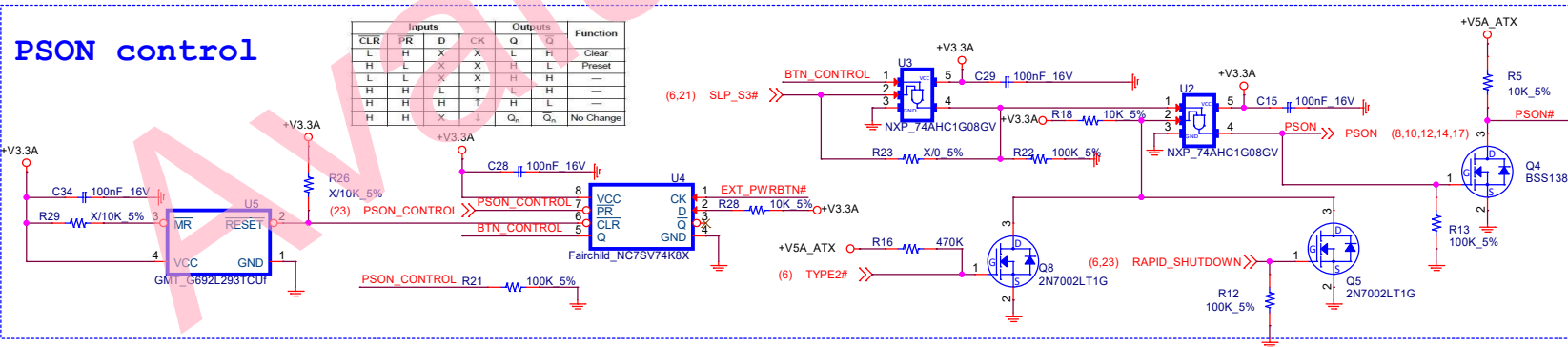
+V3.3A



Discharge circuit



PSON control



Modify History

EEV-EX16 Rev:A0

EE:Gas

Item	Description	Track or reason	Page	Date
1.	First Release			

EEV-EX16 Rev:A01

EE:Elmo

Item	Description	Track or reason	Page	Date
1.	E1907EX1601RO Release	PCB Part Number Update.	06	2019/10/23
2.	CN1#3~12	Nut and Column BOM Level Change to DIP.	06	2019/10/23
3.	CN1B PIN: (C19、C20、C22、C23、D19、D20、D22、D23)	PCIE HW Issue.	06	2019/10/23
4.	ADD R364、R335、334	HDMI Level Shift HDP Pull UP.	08、10、12	2019/10/23
5.	ADD B31、B32、B33、C330、C331、C332	VGA EMI Issus.	14	2019/10/23
6.	Change U21、U31、U37、U41	USB Protect IC Change to APL3553.	17	2019/10/23
7.	Change R312、R353、R381、R458	USB Delay Resistor Change.	17	2019/10/23
8.	Enable : +V5_USB45_IN 、+V5S	USB Protect IC Change Enable POWER.	17	2019/10/23
9.				2019/10/23

EEV-EX16 Rev:A1

EE:Elmo

Item	Description	Track or reason	Page	Date
1.	Remove R373 , Add R386	USB45 use Standby Power.	17	2020/05/21
2.	Remove Q33 U40 , Add R452	LAN ACT Control.	18	2020/05/21
3.	Remove IET_CB1	Final Bom Cost Down.	21	2020/05/21
4.	Remove C253 C254 C263 C264 C273 C274 , Add R493 R494 R495 R496 R497 R498	DP Issue.	07、09、11	2020/05/21