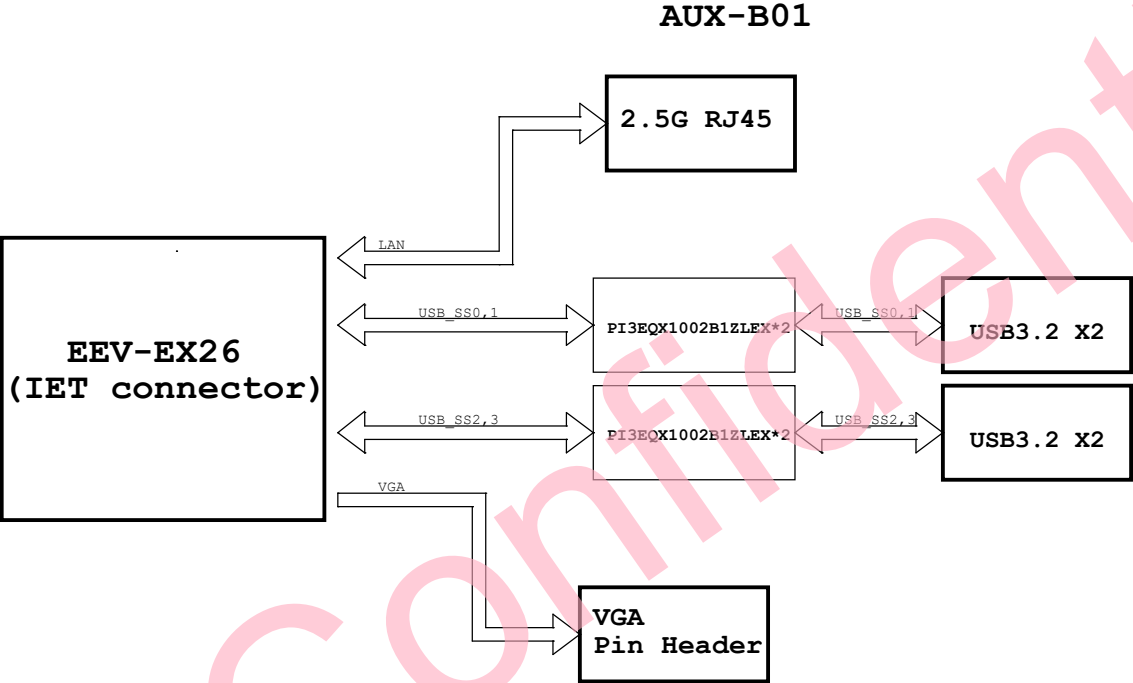


Page	Function
01	BLOCK DIAGRAM
02	Power Delivery Map
03	Clock Distribution
04	Power Sequence
05	Board information
06	IET,2.5G LAN
07	USB 3.2 Gen2 0,1
08	USB 3.2 Gen2 2,3
09	VGA
10	MODIFY HISTORY

BLOCK DIAGRAM



Power Delivery Map

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Project Name AUX-B01		Module Number ?	Rev ?
Size A3	Title Power Delivery Map		Rev A0
Date: Thursday, September 26, 2024		Sheet 2 of 10	



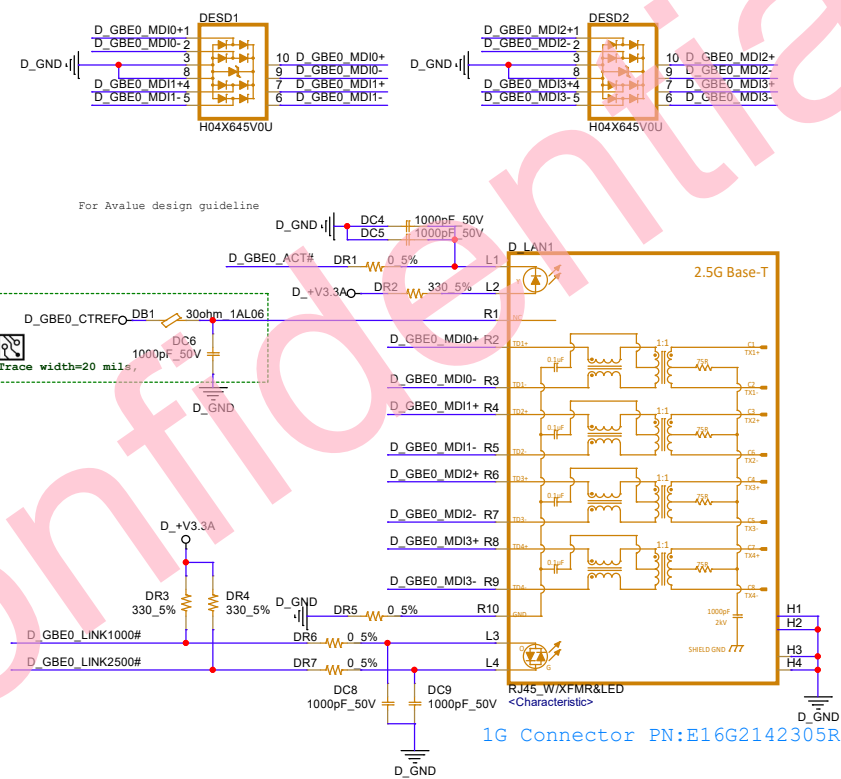
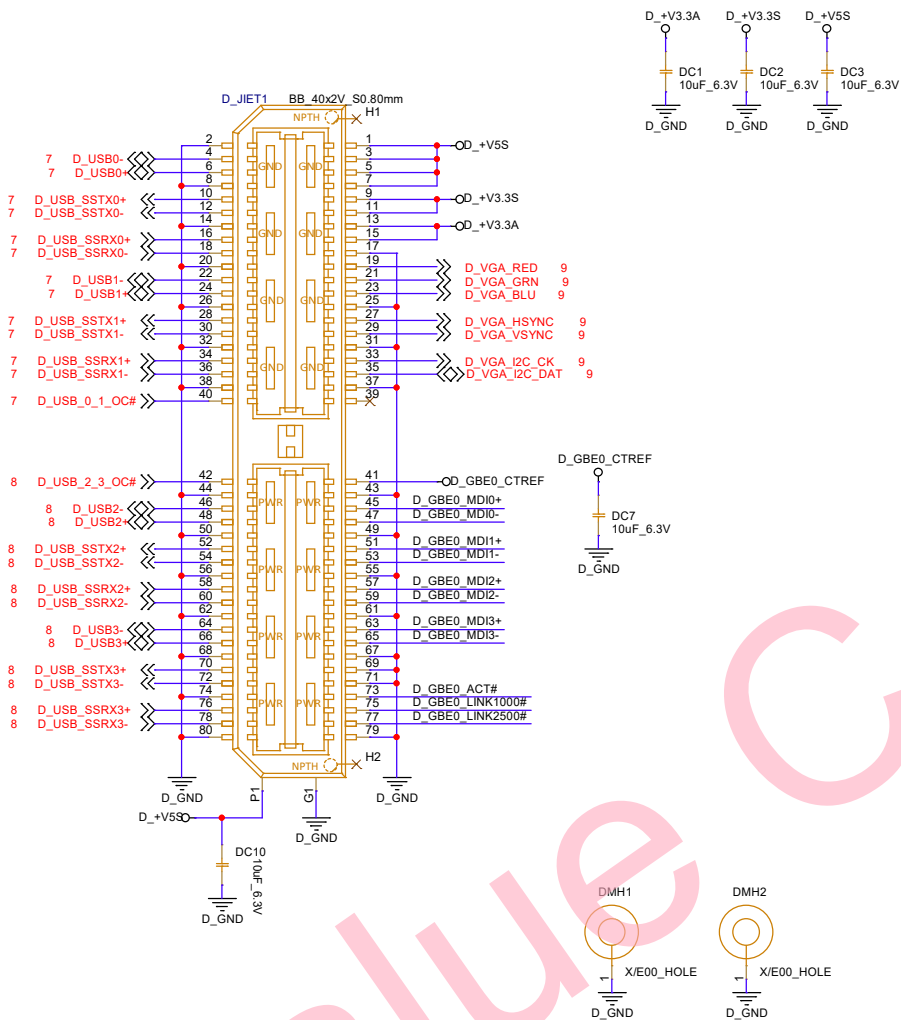
Power Sequence

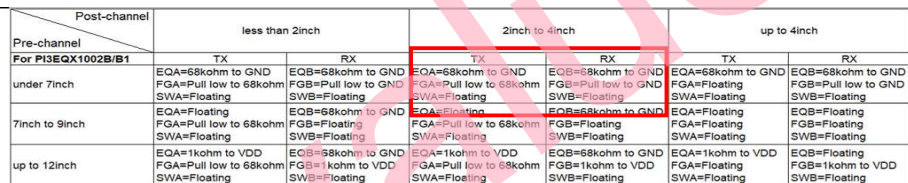
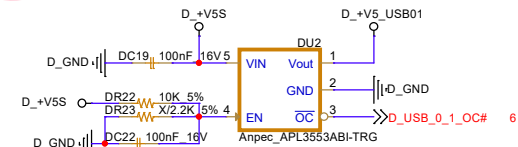
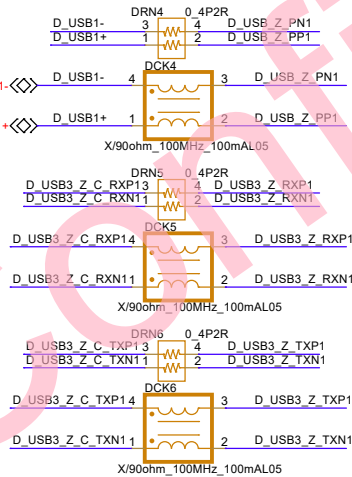
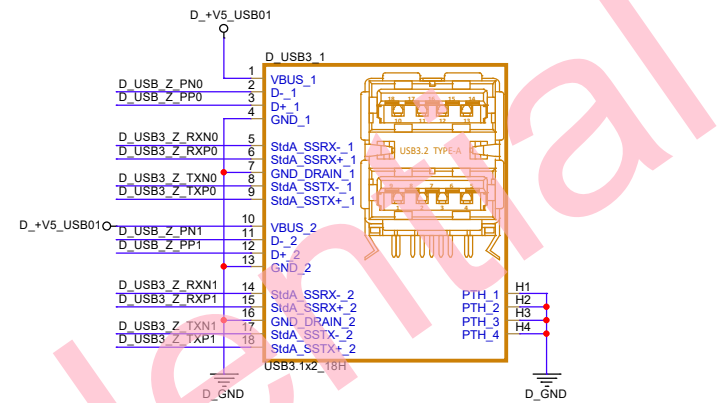
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Project Name AUX-B01		Module Number ?	Rev ?
Size A3	Title Power Sequence		Rev A0
Date: Thursday, September 26, 2024		Sheet 4 of 10	

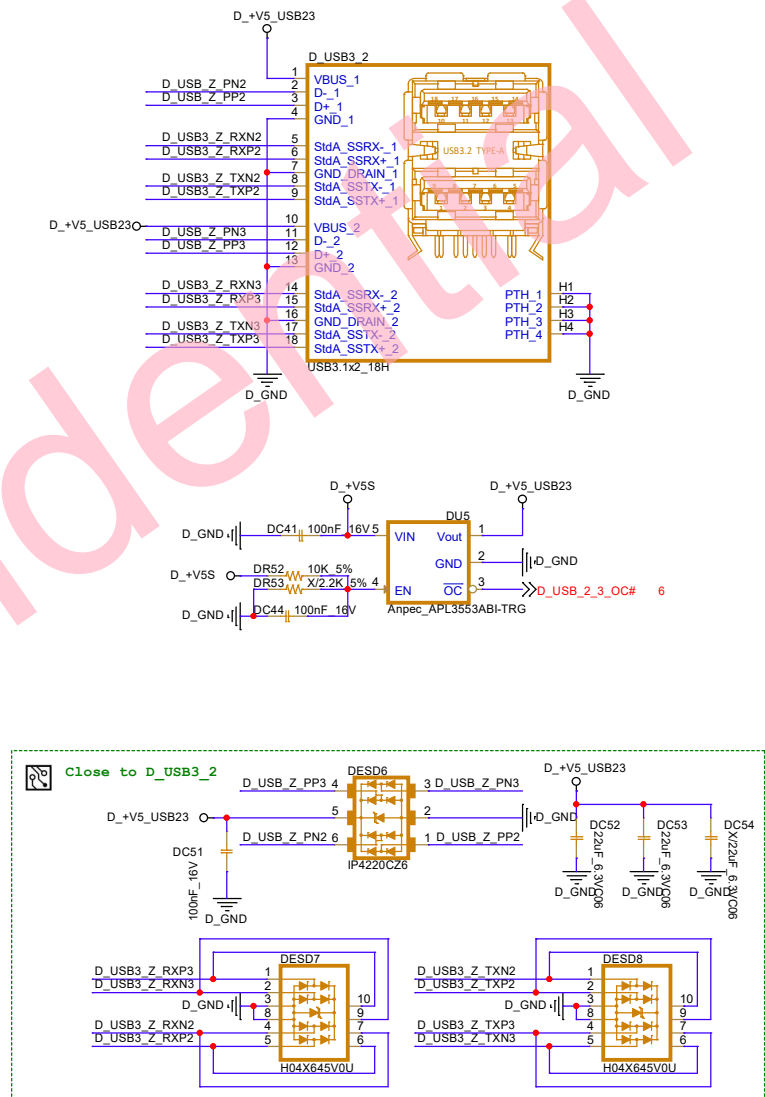
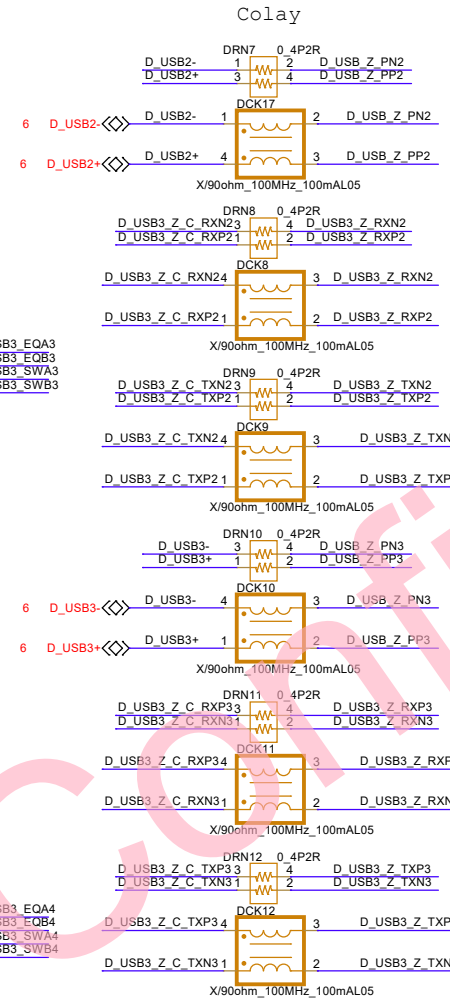
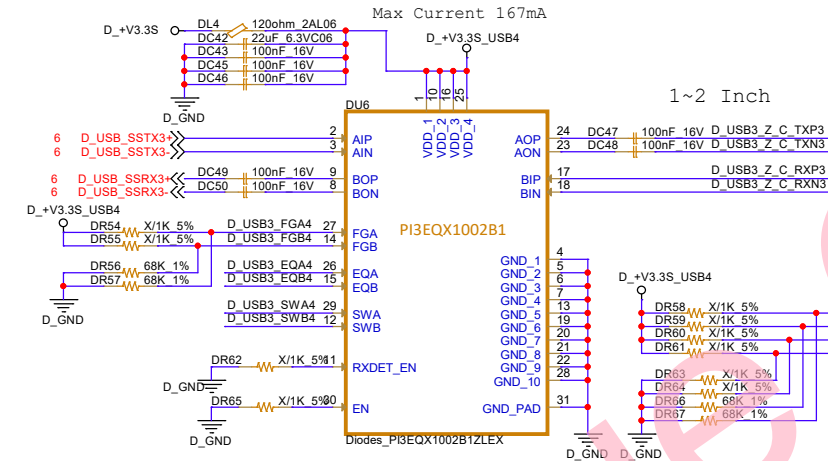
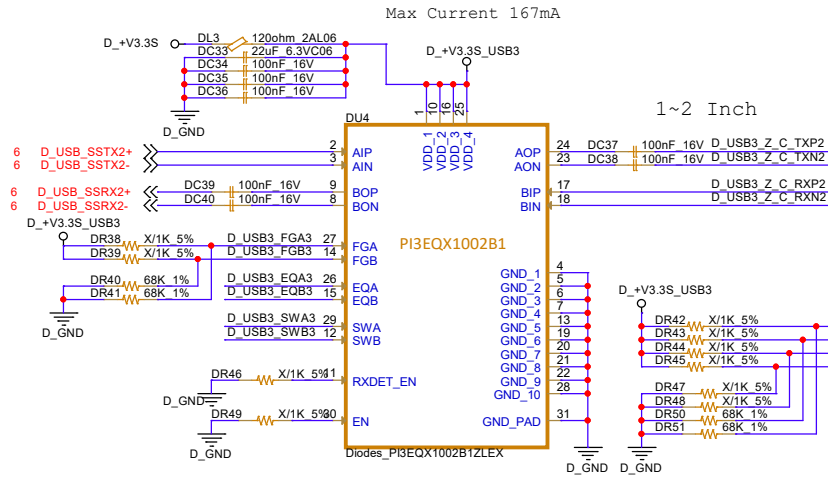


		Confidential	
Project Name AUX-B01		Module Number ?	Rev ?
Size A3	Title Board information		Rev A0
Date: Thursday, September 26, 2024		Sheet 5 of 10	



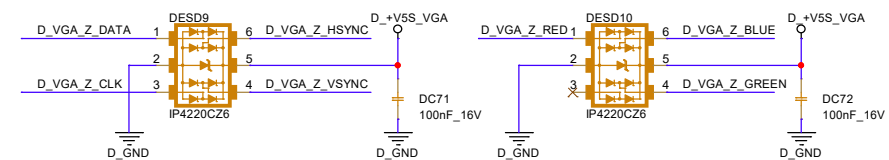
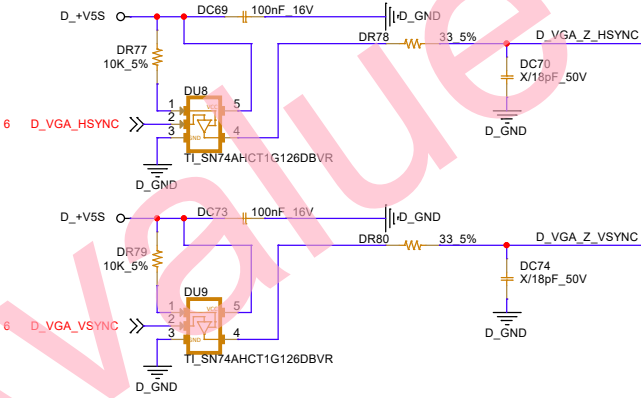
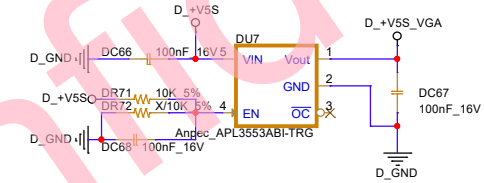
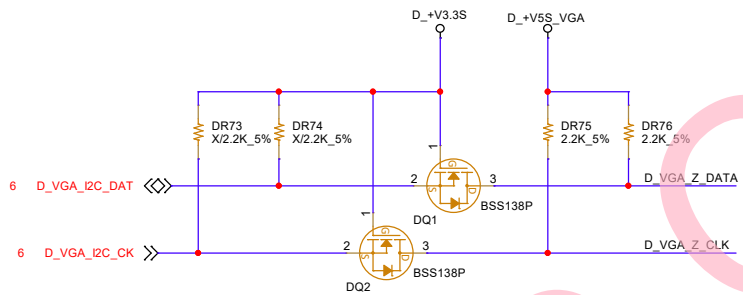
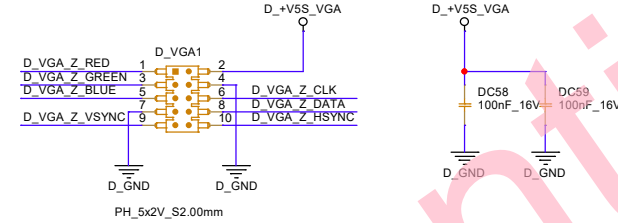
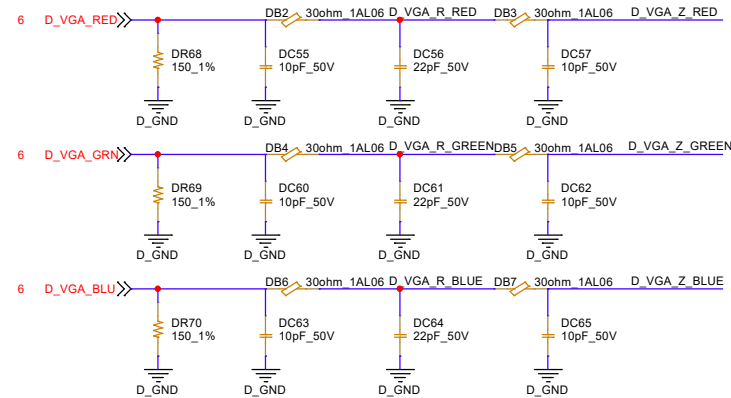


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Project Name AUX-B01		Module Number ?	
Size A3	File USB3.2	Revision A0	
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	Post-channel	less than 2inch	2inch to 4inch	up to 4inch
For PI3EQX1002B/B1				
Pre-channel				
under 7inch				
7inch to 9inch				
up to 12inch				

Table2: PCB Trace vs PI3EQX1002B/B1 ReDriver Setting



Modify History

AUX-B01 Rev:A0

EE:Tony

Item	Description	Track or reason	Page	Date
1.	First Release			2024/09/26

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