



# **Intel Atom® x6000E series Industrial Non-FuSa Silicon, and Intel Pentium® and Celeron® N and J Series processors (Formerly known as Elkhart Lake) Platform CRB Intel® Safety Island (Intel® SI) Firmware**

**Revision 048B**

**Release Notes**

---

***March 2021***

***Intel Confidential***



You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or visit [www.intel.com/design/literature.htm](http://www.intel.com/design/literature.htm).

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No product or component can be absolutely secure. Check with your system manufacturer or retailer or learn more at [intel.com](http://intel.com).

No product or component can be absolutely secure.

Intel and the Intel logo are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries.

\*Other names and brands may be claimed as the property of others.

© Intel Corporation

Intel Atom® x6000E series Industrial,  
Non-FuSa Silicon and Intel Pentium®  
and Celeron® N and J Series processors  
(Formerly known as Elkhart Lake)  
Platform CRB Intel® Safety Island (Intel® SI) Firmware  
Release Notes

Contents

1.0	Introduction .....	5
1.1	Intended Audience.....	5
1.2	Customer Support.....	5
1.3	Terminology.....	5
1.4	Reference Documents .....	5
2.0	Intel® Safety Island .....	6

Tables

Table 1.	Terminology.....	5
Table 2.	Reference Documents .....	5
Table 3.	Intel® Safety Island.....	6



## Revision History

---

Date	Revision	Description
March 2021	048B	Production Version Release
January 2021	048B	Pre-Production QS Release
December 2020	048B	Beta 4 Engineering Release
September 2020	045A	Beta 1 and 2 Release, Beta 3 Engineering Release
July 2020	042	Alpha 8 Release
March 2020	036A	Alpha 1, Alpha 3, Alpha 5 Release
December 2019	033A	Engineering Release 3 (ER3)
November 2019	031	Engineering Release 1 (ER1)
October 2019	028	Engineering Release 0 (ER0)
August 2019	025	Pre-Silicon Software External Release 23 (ER23)
June 2019	020	Pre-Silicon Software External Release 20 (ER20)

§

## 1.0 Introduction

---

### 1.1 Intended Audience

This document is intended for Intel IOTG customers. This package contains the ISI firmware binary. This package is available to Intel customers who have an agreement in place to use Intel production products.

### 1.2 Customer Support

For technical support, go to Intel® Premier Support:  
<https://employeeportal.intel.com/irj/portal/IntelPremierSupportUser>

### 1.3 Terminology

Table 1. Terminology

Term	Description
Intel® SI	Intel® Safety Island

### 1.4 Reference Documents

Table 2. Reference Documents

Document	Document No.
<i>Elkhart Lake FuSa User Guide</i>	610113

§

## 2.0 Intel® Safety Island

Table 3. Intel® Safety Island

Intel® Safety Island Version	Change Summary	Known Issues/Limitation
ISI_FW_R048B.bin	<ul style="list-style-type: none"> <li>Fixed software adaptation for ClockMon rework and ISI register alignment.</li> </ul>	<ul style="list-style-type: none"> <li>FRCPU mailbox interrupt.</li> <li>FSTM does not trigger PLL and VID FST periodically.</li> </ul>
ISI_FW_R045A.bin	<ul style="list-style-type: none"> <li>Fixed VID/DT CRC mismatch failure.</li> <li>Fixed issue for communication over SPI with 4 wire on MCU setup.</li> </ul>	<ul style="list-style-type: none"> <li>Alert is asserted only once when multiple warn alarms occur simultaneously.</li> <li>Host is not notified when loopback mismatch occurs for NOK and alert assertion.</li> <li>Firmware hangs when injecting PSS parity error.</li> <li>Some error codes not reported by ISI to Host.</li> </ul>
ISI_FW_R042.bin	<ul style="list-style-type: none"> <li>Changed TIMER_TICKS_PER_MICRO_SEC calculation in timer modules to avoid division operation.</li> </ul>	<ul style="list-style-type: none"> <li>BSP to be fixed in code.</li> <li>RTOS, GP, Periodic and WD Timer driver issues.</li> </ul>
ISI_FW_R036A.bin	<ul style="list-style-type: none"> <li>Clock monitoring and FrCPU are enabled.</li> </ul>	<ul style="list-style-type: none"> <li>Proof test is disabled.</li> <li>ODCC 1002D is not enabled.</li> <li>VID and Punit features are disabled.</li> </ul>
ISI_FW_R033A.bin	N/A	N/A
ISI_FW_R031.bin	N/A	N/A
ISI_FW_R028.bin	N/A	N/A
ISI_FW_R020.bin	N/A	N/A

§